R13 INTEL UMA/DISCRETE SYSTEM DIAGRAM 01

+3V/+5V S5 PG.31
+1.05V_VTT PG.32
CPU Core PG.33~34
DDR3 PG.35
VCCSA PG.36
Charge PG.37
+VGACORE PG.39

SODIMM1 Max. 4GB PG.12 — DDR3 Channel A
SODIMM2 Max. 4GB PG.13 — DDR3 Channel B

INTEL Sandy
37.5mm X 37.5mm
989pin PGA
TDP 35W
PG.2~5

PCI-E x8

AMD Seymour
23mm X 23mm
TDP 15W
PG.14~18

DDR3 800MHz
VRAM 64Mx16x4,64bit PG.19

HDMI PG.21
CRT PG.22
LVDS PG.20

FDI
DMI

HDD PG.23 — SATA0
ODD PG.23 — SATA1

INTEL PCH
COUGAR POINT
PG.6~11

DP Port B
CRT
LVDS

PCI-E x 1
LANE1
LANE0

LAN
RTL8165EH
10/100
PG.27

WLAN
BT COMBO
PG.30
USB 2.0
PORT10

USB2.0 Ports X3 PG.26
PORT0,1,8

Webcam PG.20
PORT4

USB 2.0
PORT13

BT
Softbreeze
PG.26

PCI-E x 1
LANE2

Card Reader
RTS5219
PG.24

KBC
EnE KB3930QF A1 PG.29
LPC

KB
TP
ROM
FAN

AUDIO CODEC
IDT 92HD80Bx
PG.25

Speaker PG.25
HP/MIC PG.26
Analog MIC PG.25

Stackup
TOP
GND
IN1
IN2
VCC
BOT

NB5

PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Saturday, September 18, 2010 Sheet 1 of 39

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Sandy Bridge Processor (DMI,PEG,FDI)

Sandy Bridge Processor (CLK,MISC,JTAG)

02

U15A

DMI_TXN0 6 → B27 DMI_RX#[0]
DMI_TXN1 6 → B25 DMI_RX#[1]
DMI_TXN2 6 → A25 DMI_RX#[2]
DMI_TXN3 6 → B24 DMI_RX#[3]

DMI_TXP0 6 → B28 DMI_RX[0]
DMI_TXP1 6 → B26 DMI_RX[1]
DMI_TXP2 6 → A24 DMI_RX[2]
DMI_TXP3 6 → B23 DMI_RX[3]

DMI_RXN0 6 → G21 DMI_TX#[0]
DMI_RXN1 6 → E22 DMI_TX#[1]
DMI_RXN2 6 → F21 DMI_TX#[2]
DMI_RXN3 6 → D21 DMI_TX#[3]

DMI_RXP0 6 → G22 DMI_TX[0]
DMI_RXP1 6 → D22 DMI_TX[1]
DMI_RXP2 6 → F20 DMI_TX[2]
DMI_RXP3 6 → C21 DMI_TX[3]

DMI

FDI_TXN0 6 → A21 FDI0_TX#[0]
FDI_TXN1 6 → H19 FDI0_TX#[1]
FDI_TXN2 6 → E19 FDI0_TX#[2]
FDI_TXN3 6 → F18 FDI0_TX#[3]
FDI_TXN4 6 → B21 FDI1_TX#[0]
FDI_TXN5 6 → C20 FDI1_TX#[1]
FDI_TXN6 6 → D18 FDI1_TX#[2]
FDI_TXN7 6 → E17 FDI1_TX#[3]

FDI_TXP0 6 → A22 FDI0_TX[0]
FDI_TXP1 6 → G19 FDI0_TX[1]
FDI_TXP2 6 → E20 FDI0_TX[2]
FDI_TXP3 6 → G18 FDI0_TX[3]
FDI_TXP4 6 → B20 FDI1_TX[0]
FDI_TXP5 6 → C19 FDI1_TX[1]
FDI_TXP6 6 → D19 FDI1_TX[2]
FDI_TXP7 6 → F17 FDI1_TX[3]

FDI_FSYNC0 6 → J18 FDI0_FSYNC
FDI_FSYNC1 6 → J17 FDI1_FSYNC

FDI_INT 6 → H20 FDI_INT

FDI_LSYNC0 6 → J19 FDI0_LSYNC
FDI_LSYNC1 6 → H17 FDI1_LSYNC

Intel(R) FDI

eDP_COMP → A18 eDP_COMPIO
INT_eDP_HPD_Q → A17 eDP_ICOMPO
B16 eDP_HPD

C15 eDP_AUX
D15 eDP_AUX#

C17 eDP_TX[0]
F16 eDP_TX[1]
C16 eDP_TX[2]
G15 eDP_TX[3]

C18 eDP_TX#[0]
E16 eDP_TX#[1]
D16 eDP_TX#[2]
F15 eDP_TX#[3]

eDP

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000005
IC SOCKET RPGA 989P(P1.0,M/H3.0)

eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.

PCI EXPRESS* - GRAPHICS

PEG_ICOMPI J22 → PEG_COMP
PEG_ICOMPO J21
PEG_RCOMPO H22

PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

PEG_RX#[0..7] 14 → K33 PEG_RX#0, M35 PEG_RX#1, L34 PEG_RX#2, J35 PEG_RX#3, J32 PEG_RX#4, H34 PEG_RX#5, H31 PEG_RX#6, G33 PEG_RX#7

PEG_RX#[0] F35
PEG_RX#[1] E34
PEG_RX#[2] E32
PEG_RX#[3] D33
PEG_RX#[4] D31
PEG_RX#[5] B33
PEG_RX#[6] C32
PEG_RX#[7] G30
PEG_RX#[8] F30
PEG_RX#[9] E35
PEG_RX#[10] E33
PEG_RX#[11] F32
PEG_RX#[12] D34
PEG_RX#[13] E31
PEG_RX#[14] C33
PEG_RX#[15] B32

PEG_RX[0..7] 14 → J33 PEG_RX0, L35 PEG_RX1, K34 PEG_RX2, H35 PEG_RX3, H32 PEG_RX4, G34 PEG_RX5, G31 PEG_RX6, E33 PEG_RX7

PEG_TX#[0] M29 → C_PEG_TX#0
PEG_TX#[1] M32 → C_PEG_TX#1
PEG_TX#[2] M31 → C_PEG_TX#2
PEG_TX#[3] L32 → C_PEG_TX#3
PEG_TX#[4] L29 → C_PEG_TX#4
PEG_TX#[5] K31 → C_PEG_TX#5
PEG_TX#[6] K28 → C_PEG_TX#6
PEG_TX#[7] J30 → C_PEG_TX#7
PEG_TX#[8] J28
PEG_TX#[9] H29
PEG_TX#[10] G27
PEG_TX#[11] E29
PEG_TX#[12] F27
PEG_TX#[13] D28
PEG_TX#[14] F26
PEG_TX#[15] E25

PEG_TX[0] M28 → C_PEG_TX0
PEG_TX[1] M33 → C_PEG_TX1
PEG_TX[2] M30 → C_PEG_TX2
PEG_TX[3] L31 → C_PEG_TX3
PEG_TX[4] L28 → C_PEG_TX4
PEG_TX[5] K30 → C_PEG_TX5
PEG_TX[6] K27 → C_PEG_TX6
PEG_TX[7] J29 → C_PEG_TX7
PEG_TX[8] J27
PEG_TX[9] H28
PEG_TX[10] G28
PEG_TX[11] E28
PEG_TX[12] F28
PEG_TX[13] D27
PEG_TX[14] E26
PEG_TX[15] D25

U15B

H_SNB_IVB# 7 → C26 SNB_IVB#
SNB_IVB# N.A at SNB EDS #27637 0.7v1
TP4 SKTOCC# → AN34 SKTOCC#

MISC

TP2 TP_CATERR# → AL33 CATERR#

Placement close to EC.

EC_PECI 29 → R386 43_4 H_PECI → AN33 PECI
H_PROCHOT# 29,33 → R146 56.2/F_4 H_PROCHOT#_R → AL32 PROCHOT#
PM_THRMTRIP# 9,29 → R148 0_4 PM_THRMTRIP#_R → AN32 THERMTRIP#

THERMAL

PM_SYNC 6 → R377 0_4 PM_SYNC_R → AM34 PM_SYNC
H_PWRGOOD 9 → R378 0_4 H_PWRGOOD_R → AP33 UNCOREPWRGOOD
R384 10K_4
PM_DRAM_PWRGD_R V8 → SM_DRAMPWROK
RESET# ← AR33 CPU_PLTRST#_R ← R400 *43_4 ← R404 *75/F_4 ← +1.05V_VTT
CPU_PLTRST# ← U18 GND OUT, IN, NC VCC *74LVC1G07GW ← +3VS5, C560 0.1U/10V_4
8,14,24,27,29,30 PLTRST# → U18 IN
R401 750/F_4
R402 1.5K/F_4

PWR MANAGEMENT

9/15 SI for H/W.

CPU RESET#

SM_DRAMPWROK Processor Input.

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000005
IC SOCKET RPGA 989P(P1.0,M/H3.0)

CLOCKS

BCLK A28 → CLK_CPU_BCLKP 8
BCLK# A27 → CLK_CPU_BCLKN 8
DPLL_REF_SSCLK A16 → CLK_DPLL_SSCLKP
DPLL_REF_SSCLK# A15 → CLK_DPLL_SSCLKN

DDR3 MISC

SM_DRAMRST# → R8 CPU_DRAMRST#
SM_RCOMP[0] AK1 → SM_RCOMP_0 R143 140/F_4
SM_RCOMP[1] A5 → SM_RCOMP_1 R318 26.1/F_4
SM_RCOMP[2] A4 → SM_RCOMP_2 R316 200/F_4

SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,

JTAG & BPM

CPU XDP

PRDY# AP29 → XDP_PRDY# → TP12
PREQ# AP27 → XDP_PREQ# → TP11
TCK AR26 → XDP_TCLK → TP8
TMS AR27 → XDP_TMS → TP10
TRST# AP30 → XDP_TRST# → TP13
TDI AR28 → XDP_TDI_R → TP39
TDO AP26 → XDP_TDO → TP7
DBR# AL35 → XDP_DBRST# → R375 *1K_4 → +3V
XDP_DBRST# 6
BPM#[0] AT28 → XDP_BPM0 → TP40
BPM#[1] AR29 → XDP_BPM1 → TP41
BPM#[2] AR30 → XDP_BPM2 → TP43
BPM#[3] AT30 → XDP_BPM3 → TP42
BPM#[4] AP32 → XDP_BPM4 → TP5
BPM#[5] AR31 → XDP_BPM5 → TP45
BPM#[6] AT31 → XDP_BPM6 → TP44
BPM#[7] AR32 → XDP_BPM7 → TP46

DDR3 DRAM RESET

+1.5VSUS → R311 1K_4 → R313 *0_4
12,13 DDR3_DRAMRST# → R312 1K_4 → Q24 2N7002 → CPU_DRAMRST#
CPU_DRAMRST#_R
8 DRAMRST_CNTRL_PCH → R315 0_4
C442 0.047U/10V_4
R314 4.99K/F_4

+3VS5 → R49 10K_4 → PM_DRAM_PWRGD_PU
U2 NC VCC, IN, GND OUT *74LVC1G07GW
PM_DRAM_PWRGD_C → R37 *39_4 → PM_DRAM_PWRGD_R → R42 130/F_4 → R40 200/F_4 → +1.5V_CPU
C27 0.1U/10V_4
R48 *0_4 → PM_DRAM_PWRGD 6
R47 0_4 → PM_DRAM_PWRGD_R
R43 *3K/F_4
Q3 *2N7002 → MAIN_ONG 4,38

+1.05V_VTT 4,6,7,8,10,29,32,33
+1.5V_CPU 4
+3VS5 6,7,8,9,10,22,26,31,32,38,39
+3V 6,7,8,9,10,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,38,39

FDI disable (DIS only stuff)

DEL

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

PEG x16 disable (UMA only remove)

14 PEG_TX[0..7]

C_PEG_TX0	C483	0.1U/10V_4	PEG_TX0
C_PEG_TX1	C489	0.1U/10V_4	PEG_TX1
C_PEG_TX2	C492	0.1U/10V_4	PEG_TX2
C_PEG_TX3	C498	0.1U/10V_4	PEG_TX3
C_PEG_TX4	C501	0.1U/10V_4	PEG_TX4
C_PEG_TX5	C504	0.1U/10V_4	PEG_TX5
C_PEG_TX6	C508	0.1U/10V_4	PEG_TX6
C_PEG_TX7	C512	0.1U/10V_4	PEG_TX7

14 PEG_TX#[0..7]

C_PEG_TX#0	C488	0.1U/10V_4	PEG_TX#0
C_PEG_TX#1	C490	0.1U/10V_4	PEG_TX#1
C_PEG_TX#2	C496	0.1U/10V_4	PEG_TX#2
C_PEG_TX#3	C500	0.1U/10V_4	PEG_TX#3
C_PEG_TX#4	C503	0.1U/10V_4	PEG_TX#4
C_PEG_TX#5	C507	0.1U/10V_4	PEG_TX#5
C_PEG_TX#6	C511	0.1U/10V_4	PEG_TX#6
C_PEG_TX#7	C517	0.1U/10V_4	PEG_TX#7

0.22uF AC coupling Caps for PCIE GEN1/2/3

0.22uF AC coupling Caps for PCIE GEN1/2/3

Embedded Display PLL Clock

Ra

3/26 DB change
Part reference.

CLK_DPLL_SSCLKP ← CLK_DPLL_SSCLKP 8
CLK_DPLL_SSCLKN ← CLK_DPLL_SSCLKN 8

DEL

	Ra	Rb	Rc
DIS	NC	Stuff	Stuff
SG/UMA	Stuff	NC	NC

DP & PEG Compensation

+1.05V_VTT → R67 10K_4 → INT_eDP_HPD_Q
+1.05V_VTT → R319 24.9/F_4 → eDP_COMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

+1.05V_VTT → R85 24.9/F_4 → PEG_COMP

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up (CPU)

+1.05V_VTT

H_PROCHOT#	R145	62_4
XDP_TDO	R155	51_4
XDP_TMS	R159	51_4
XDP_TDI_R	R403	51_4
XDP_PREQ#	R158	*51_4
XDP_TCLK	R156	51_4
XDP_TRST#	R163	51_4

NB5

PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 1/4 (PCIE&DMI&FDI)	3A

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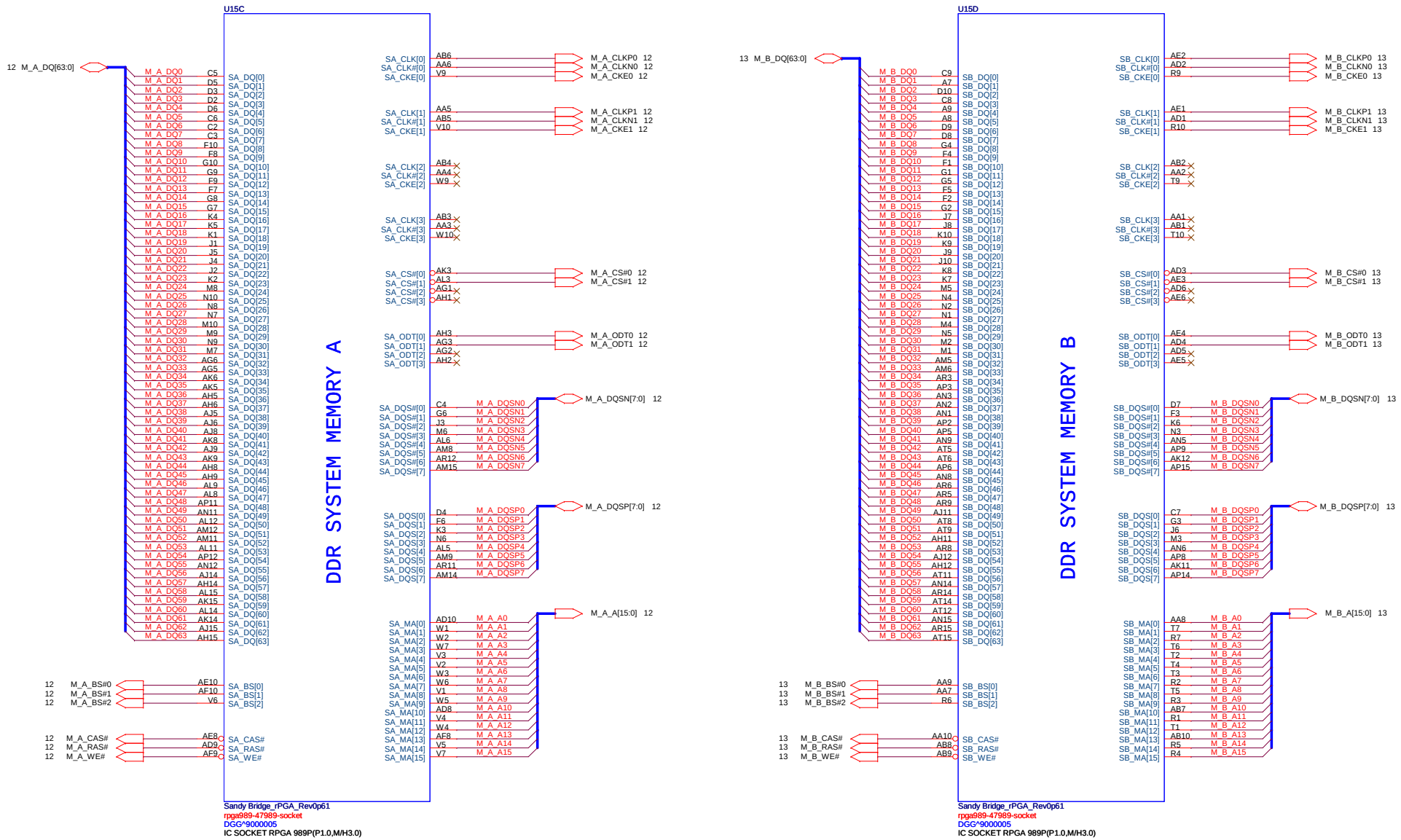
Sandy Bridge Processor (DDR3)



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PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 2/4 (DDR3 I/F)	1A

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NB5

Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

04

SNB: 55A

+VCC_CORE

U15F

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

C493 22U/6.3VS_8
C521 10U/6.3VS_6
C516 22U/6.3VS_8
C42 22U/6.3VS_8
C36 22U/6.3VS_8
C174 22U/6.3VS_8
C509 22U/6.3VS_8
C172 22U/6.3VS_8
C263 22U/6.3VS_8
C300 22U/6.3VS_8
C39 22U/6.3VS_8
C502 22U/6.3VS_8
C527 *10U/6.3V_6S
C177 22U/6.3VS_8
C33 22U/6.3VS_8
C151 22U/6.3VS_8
C286 22U/6.3VS_8
C283 22U/6.3VS_8
C237 22U/6.3VS_8
C242 22U/6.3VS_8
C163 22U/6.3VS_8
C535 *22U/6.3VS_8
C220 *22U/6.3VS_8
C447 22U/6.3VS_8
C173 22U/6.3VS_8
C515 10U/6.3VS_6
C270 22U/6.3VS_8
C450 22U/6.3VS_8
C451 22U/6.3VS_8
C542 *10U/6.3V_6S

22uF_8 x8 Socket TOP cavity
22uF_8 x10 Socket BOT cavity
22uF_8 x8 Socket TOP edge
470uF_7343 x4

3/26 DB change 10U FP to 0805.

+VCC_CORE 22,34
+VCC_GFX 34
+VCCSA 36
+1.05V_VTT 2,6,7,8,10,29,32,33
+1.5V_CPU 2
+1.5V_CPU 2
+1.5VSUS 2,10,12,13,22,35,39

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000005
IC SOCKET RPGA 989P(P1.0,M/H3.0)

SNB: 8.5A

+1.05V_VTT

C145 22U/6.3VS_8
C147 22U/6.3VS_8
C482 22U/6.3VS_8
C260 22U/6.3VS_8
C180 22U/6.3VS_8
C166 22U/6.3VS_8
C146 *22U/6.3VS_8
C215 22U/6.3VS_8
C526 22U/6.3VS_8
C532 *22U/6.3VS_8
C200 *22U/6.3VS_8
C61 *22U/6.3VS_8
5/14 modify
C491 22U/6.3VS_8
C66 *22U/6.3VS_8
C282 *22U/6.3VS_8
C167 *22U/6.3VS_8
C506 22U/6.3VS_8
C236 *22U/6.3VS_8
C513 *22U/6.3VS_8
C499 22U/6.3VS_8
C158 22U/6.3VS_8

22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

+1.05V_VTT
+1.05V_VTT_40 R86 *0_4/S

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 H_CPU_SVIDCLK
VIDSOUT AJ28 H_CPU_SVIDDAT

R136 100_4 +VCC_CORE
VCC_SENSE AJ35 VCC_SENSE 33
VSS_SENSE AJ34 VSS_SENSE 33
R139 100_4

VCCIO_SENSE B10 VCCP_SENSE 32
VSSIO_SENSE A10 VSSP_SENSE VSSP_SENSE 32

Trace Route to Power IC area.

22uF_8 x2 Socket TOP cavity
22uF_8 x2 Socket BOT cavity
22uF_8 x4 Socket TOP edge
22uF_8 x4 Socket BOT edge
470uF_7343 x2

+VCC_GFX

SNB: 21.5A

C529 22U/6.3V_8
C264 22U/6.3V_8
C285 22U/6.3V_8
C299 22U/6.3V_8
C284 22U/6.3V_8
C530 22U/6.3V_8
C301 22U/6.3V_8
C238 22U/6.3V_8
C528 22U/6.3V_8
C239 22U/6.3V_8
C265 22U/6.3V_8
C531 22U/6.3V_8

DEL

	DIS	SG/UMA
Ra	Stuff	NC

SNB: 1.5A

+1.8V

C449 10U/6.3V_8
C441 1U/6.3V_4
C443 1U/6.3V_4
C440 330U/2V_7343

330uF x1, 10uF_8 x1, 1uF_4 x2
Socket BOT edge.

U15G

GRAPHICS

1.8V RAIL

VCCPLL1 B6
VCCPLL2 A6
VCCPLL3 A2

VAXG_SENSE AK35
VSSAXG_SENSE AK34

SENSE LINES

R140 100_4 +VCC_GFX
VCC_AXG_SENSE 33
VSS_AXG_SENSE 33
R142 100_4

VREF

SM_VREF AL1

+VDDR_REF_CPU
CAD Note: +VDDR_REF_CPU should have 10 mil trace width
R28 *0_8 DDR_VTTREF 12,13,35
R31 100K_4
Q2 2N7002
MAIND MAIND 38

DDR3 -1.5V RAILS

VDDQ1 AF7
VDDQ2 AF4
VDDQ3 AF1
VDDQ4 AC7
VDDQ5 AC4
VDDQ6 AC1
VDDQ7 Y7
VDDQ8 Y4
VDDQ9 Y1
VDDQ10 U7
VDDQ11 U4
VDDQ12 U1
VDDQ13 P7
VDDQ14 P4
VDDQ15 P1

SNB: 5A

+1.5V_CPU

C297 10U/6.3V_6
C214 10U/6.3V_8
C289 10U/6.3V_6
C268 10U/6.3V_6

4/27: layout modify

9/10 SI for H/W.

C190 10U/6.3V_6
C305 10U/6.3V_6
C576 *330U_2.5V_5.0x5.9_ESR10m

330uF x1, 10uF_8 x6 Socket BOT edge.

SA RAIL

VCCSA1 M27
VCCSA2 M26
VCCSA3 L26
VCCSA4 J26
VCCSA5 J25
VCCSA6 J24
VCCSA7 H26
VCCSA8 H25

SNB: 6A

+VCCSA

C485 10U/6.3V_8
C448 10U/6.3V_8
C484 10U/6.3V_8
C445 *10U/6.3V_8

330uF x1, 10uF_8 x1 Socket BOT edge,
10uF_8 x2 Socket BOT cavity.

MISC

VCCSA_SENSE H23 VCCUSA_SENSE_R R82 0_4 VCCUSA_SENSE 36

FC_C22 C22 H_FC_C22 R77 10K_4
VCCSA_VID1 C24 VCCSA_SEL 36

R81 10K_4

5/11: Add for intel CRB

+1.5V_CPU R310 *0_8/S +1.5V

40mile routing

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000005
IC SOCKET RPGA 989P(P1.0,M/H3.0)

Layout note: need routing together and ALERT need between CLK and DATA.

SVID CLK

Place PU resistor close to VR
R309 *54.9/F_4 +1.05V_VTT
H_CPU_SVIDCLK VR_SVID_CLK 33

SVID DATA

+1.05V_VTT +1.05V_VTT
Place PU resistor close to CPU
R137 130/F_4
R308 *130/F_4
Place PU resistor close to VR
H_CPU_SVIDDAT VR_SVID_DATA 33

SVID ALERT

Place PU resistor close to CPU
+1.05V_VTT R26 75/F_4
H_CPU_SVIDALRT# R25 43_4 VR_SVID_ALERT# 33

+1.5VSUS +1.5V_CPU +1.5VSUS

Q36 AON7410
R185 220_8
MAIND
C438 *470P/50V_4
Q16 2N7002
MAIN_ONG 2,38

3/26 DB add for Intel. Placement close to CPU.

CPU VDDQ

NB5

PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 3/4 (POWER)	1A
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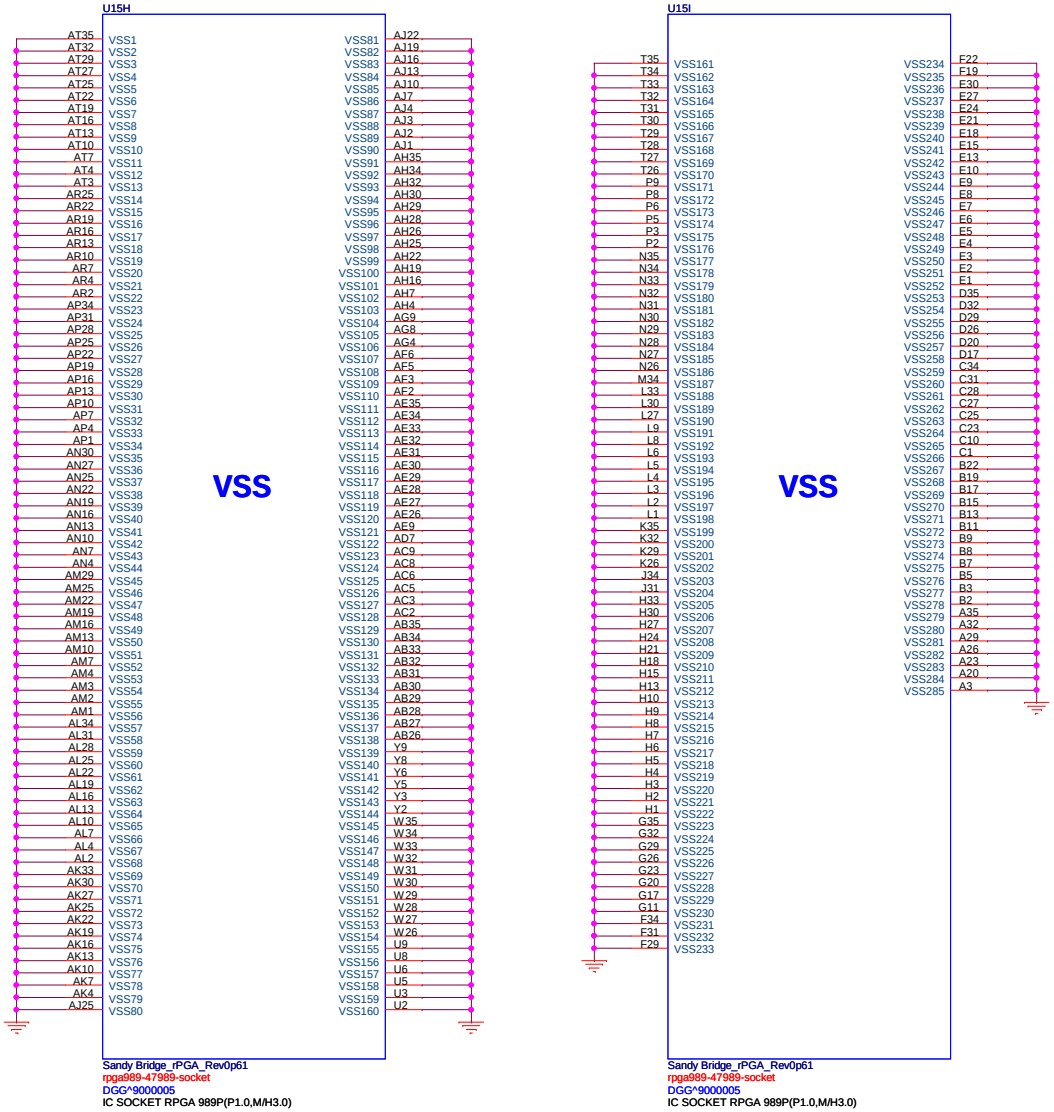
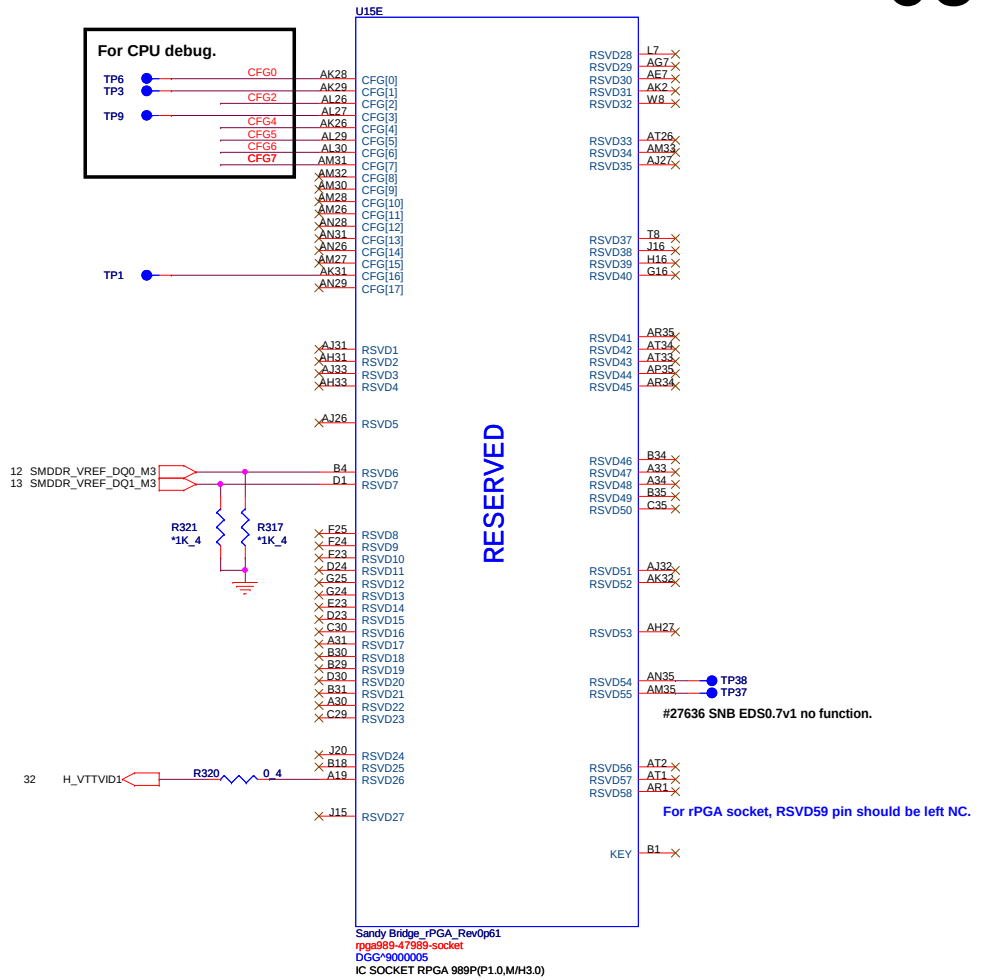
Sandy Bridge Processor (GND)



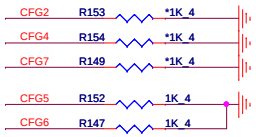
Sandy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PROJECT : R13
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	SNB 4/4 (GND)	1A

Date: Saturday, September 18, 2010 | Sheet 5 of 39

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Cougar Point (DMI,FDI,PM)

Cougar Point (LVDS,DDI)

06

U24C

U24D

DMI

FDI

System Power Management

LVDS

Digital Display Interface

CRT

INT. HDMI

9/10 SI for H/W.

PD Res place close to PCH

PCH to Res routeing 50 ohm Impedance.

Res to connector filter routeing 37.5ohm Impedance.

CougarPoint_Rev_0p7

fcbga989-intel-cougarpoint

AJ0QMZQ0T00

IC CTRL(989P)COUGARPOINT QMVY TOP B/S

9/3 SI for H/W.

Reserve for R13 power on sequence

PCH Pull-high/low(CLG)

INT HDMI disable (DIS only remove)

INT HDMI Detect Function

System PWR_OK(CLG)

On Die DSW VR Enable

High = Enable (Default)

Low = Disable

DPWROK FOR DSW

9/10 SI for EE

Remove DSW power rail

PROJECT : R13

Quanta Computer Inc.

NB5

Size: Custom | Document Number: PCH 1/6 (DMI/FDI/VIDEO) | Rev: 1A

Date: Saturday, September 18, 2010 | Sheet 6 of 39

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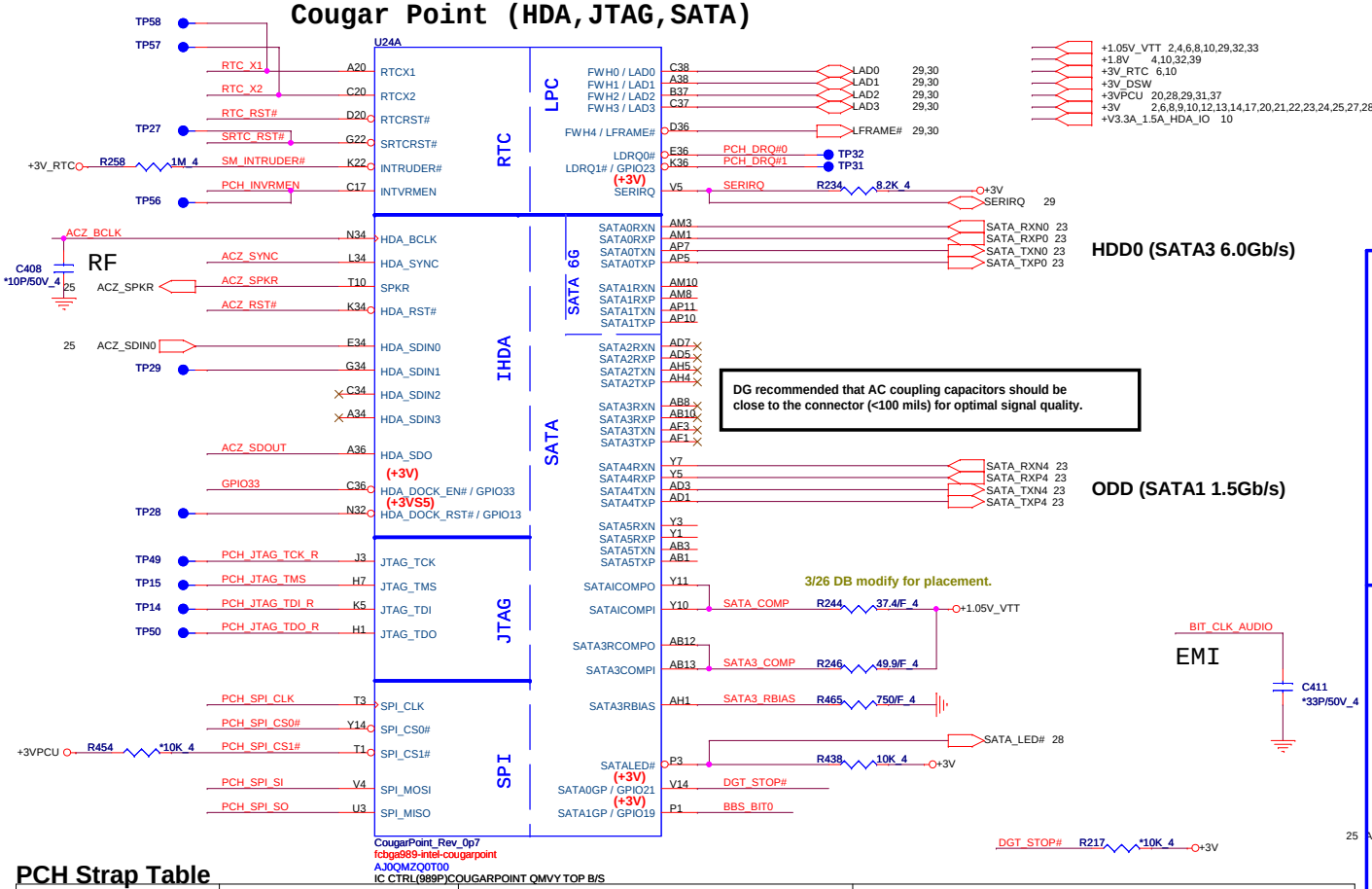
Cougar Point (HDA,JTAG,SATA)



HDD0 (SATA3 6.0Gb/s)

ODD (SATA1 1.5Gb/s)

DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

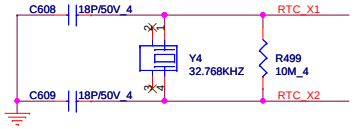
3/26 DB modify for placement.

EMI

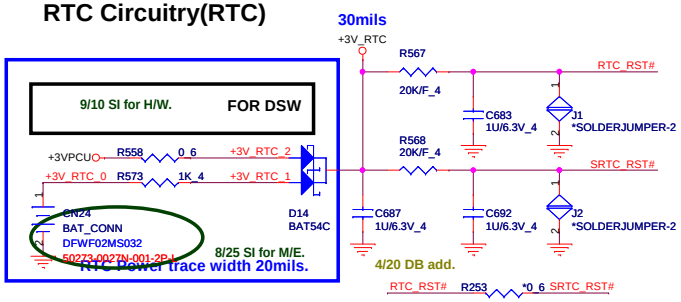
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR (Different from Calpella)	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R435 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V R522 *1K_4 R521 10K_4 PCI_GNT3# 8
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R497 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R509 1K_4 GPIO33_E 29
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# 1 0 / GNT0# 1 0 / Boot Location SPI LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GPIO19 (Different from Calpella)	Boot BIOS Selection 0 [bit-0]	PWROK		BBS_BIT0 R455 *1K_4 R523 *1K_4 BBS_BIT1 8
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R468 *1K_4 NV_ALE 8
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R470 2.2K_4 R469 4.7K_4 NV_CLE 8 H_SNB_IVB# 2 N.A at CPT EDS 0.7
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3VS5 R278 1K_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	ACZ_SDOUT R510 *1K_4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R483 *1K_4 ICC_EN# 9
GPIO28 (Different from Calpella)	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R447 *1K_4 PLL_ODVR_EN 9
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R198 1K_4 +3V

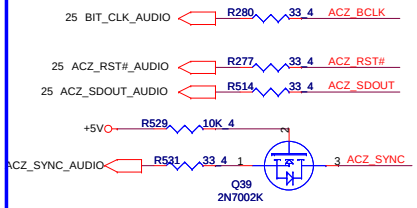
RTC Clock 32.768KHz



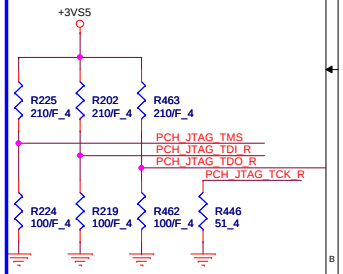
RTC Circuitry(RTC)



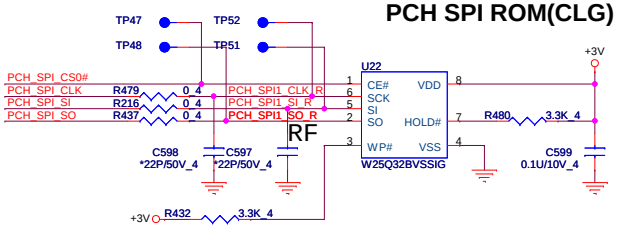
HDA Bus(CLG)



PCH JTAG Debug(CLG)



PCH SPI ROM(CLG)



Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031

PROJECT : R13
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	1A

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Cougar Point-M (PCI,USB,NVRAM)

Cougar Point-M (PCI-E,SMBUS,CLK)

08

PCI/USBOC# Pull-up(CLG)

MPC Switch Control

MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

9/3 SI for H/W.

PLTRST#(CLG)

PEG Clock detect (SG only)

SMBus/Pull-up(CLG)

CLK_REQ/Strap Pin(CLG)

PCIE Clock

SMBus/Pull-up(CLG)

change 25M to small size RF

9/8 SI for TXC

Remove Ra, Rb for UMA & SG. 27MHz support DIS only.

Remove for UMA only.

CLOCK TERMINATION for FCIM

EMI

PROJECT : R13
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PCH 3/6 (PCIE/USB/CLK)	3A

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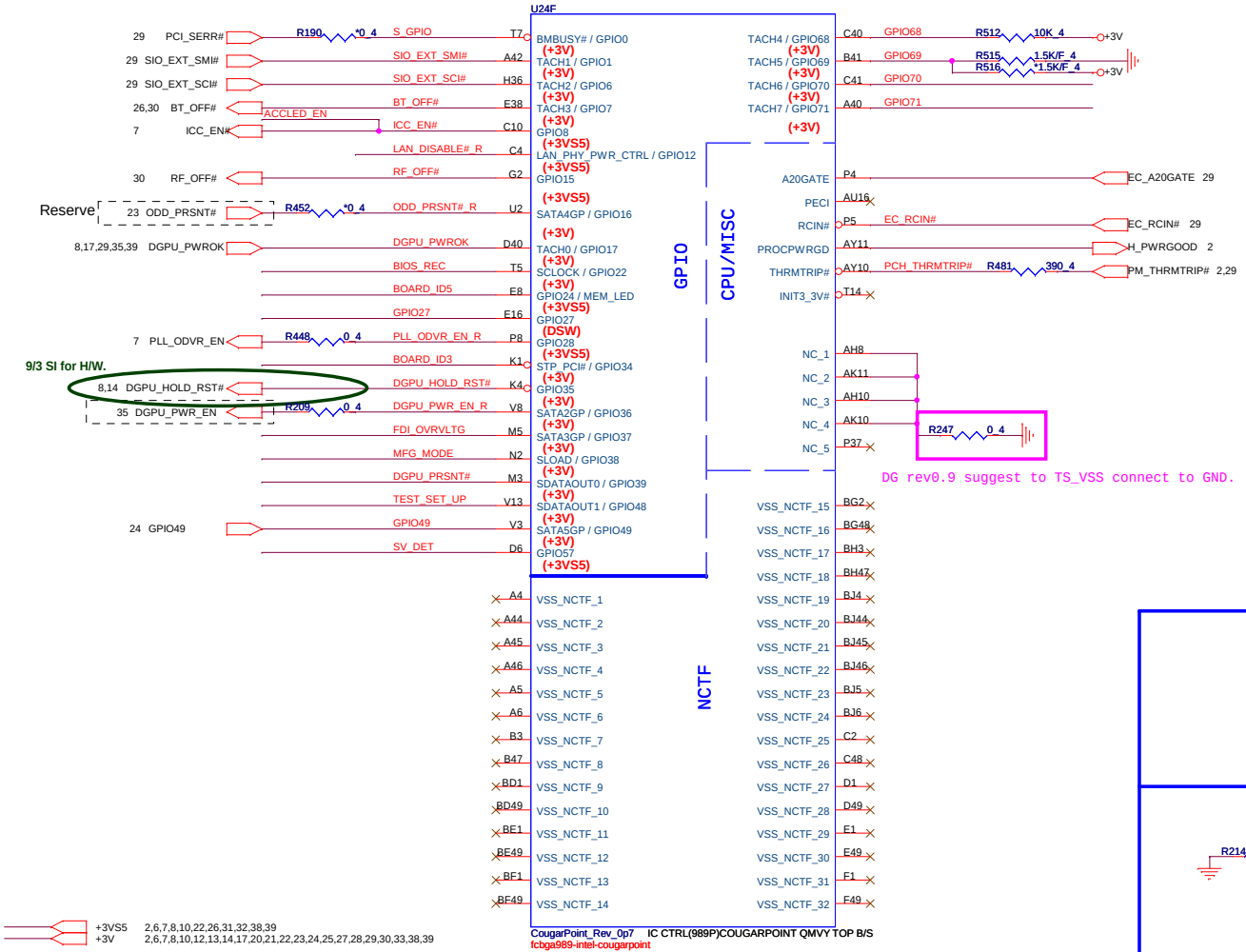
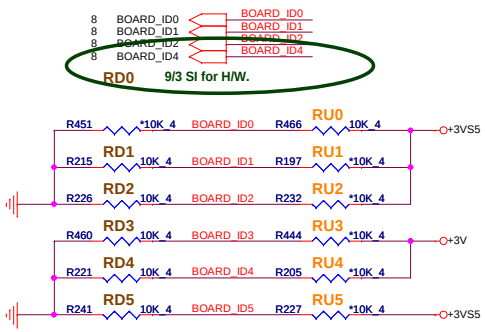
Cougar Point (GPIO,VSS_NCTF,RSVD)



BOARD ID SETTING

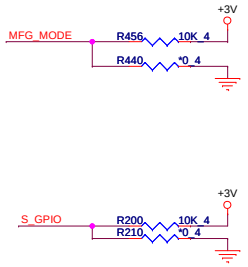
Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
R13 UMA	0	0	0	0	0	0
R13 DIS	0	0	0	0	0	1
	0	0	0	0	0	0
	0	0	0	0	0	0
	0	0	0	0	0	0



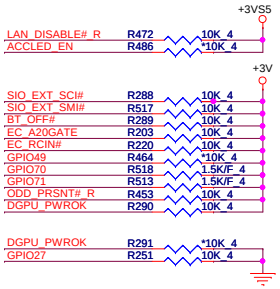
Clock Gen Power OK (CLG)

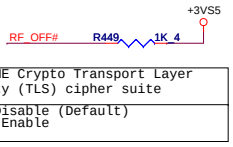
09

MFG-TEST



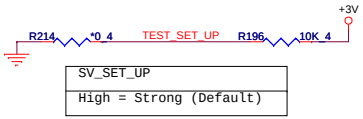
GPIO Pull-up/Pull-down(CLG)



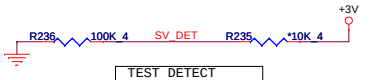


Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default) High = Enable

BIOS RECOVERY	High = Disable (Default) Low = Enable



SV_SET_UP
High = Strong (Default)

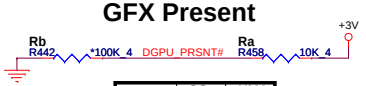


TEST DETECT
Low = Default

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

GFX Present



	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

PROJECT : R13
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	1A
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Cougar Point-M (POWER)

COUGAR POINT (POWER)

U24J

Clock and Miscellaneous | USB | PCI/GPIO/LPC | SATA | MISC | CPU | RTC | HDA

U24G

VCC CORE | CRT | LVDS | HVCMOS | VCCIO | DMI | NAND / SPI | FDI

9/10 SI for H/W.

9/15 SI for EE

UMA Only, If have power noise issue then stuff it.

U29 G910T21U

CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJ0QMZQ0T00
IC CTRL(989P)COUGARPOINT QMVY TOP B/S

+1.05V_VTT 2,4,6,7,8,29,32,33
+1.5VSUS 2,4,12,13,22,35,39
+1.8V 4,7,32,39

+3V_RTC 6,7
+3V_DSW
+3VS5 2,6,7,8,9,22,26,31,32,38,39
+3V 2,6,7,8,9,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,38,39
+5VS5 20,26,31,32,33,34,35,36,38,39
+5V 6,7,17,21,22,23,25,28,30,38

PROJECT : R13
Quanta Computer Inc.

NB5

Size: Custom | Document Number: PCH 5/6 (POWER) | Rev: 3A

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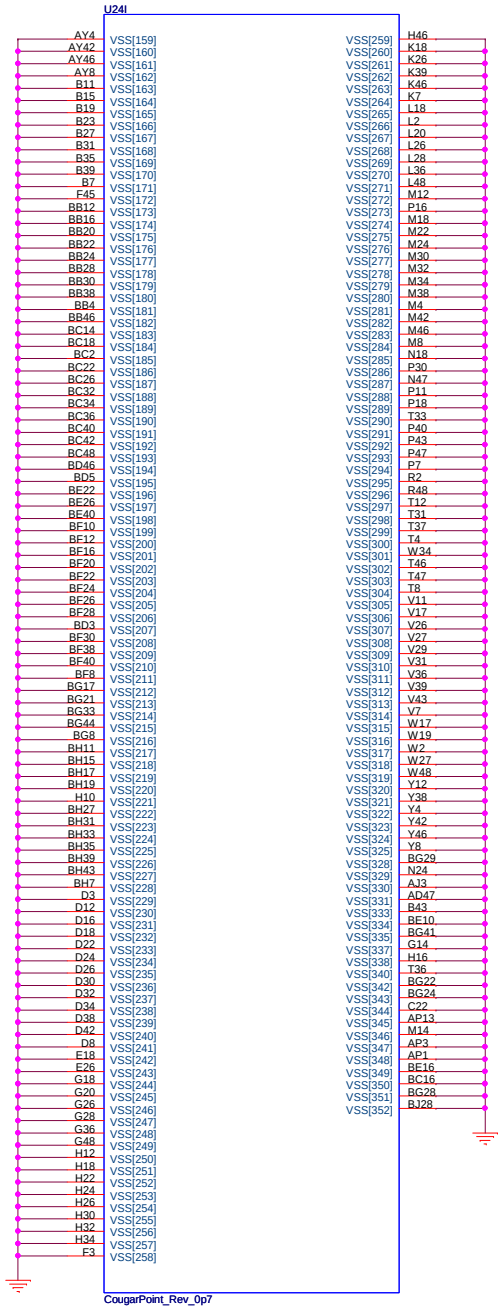
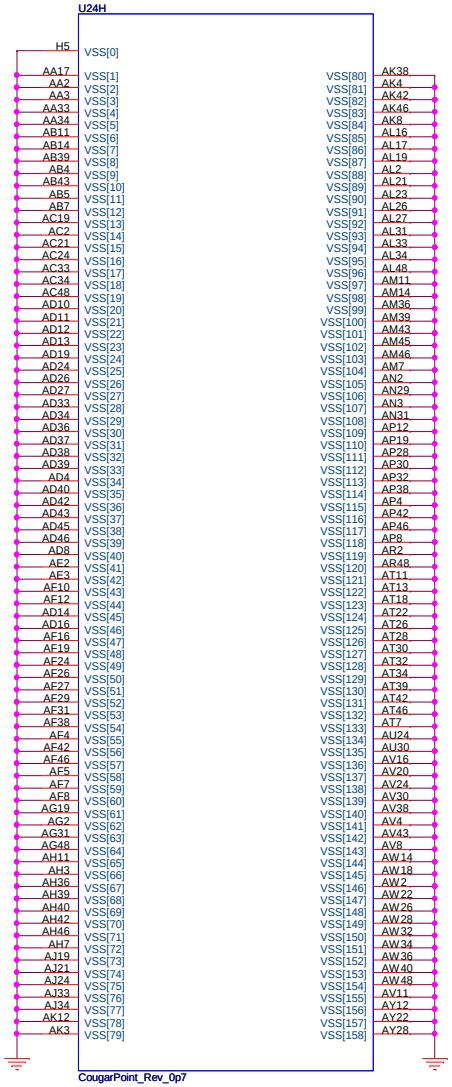
IBEX PEAK-M (GND)



IBEX PEAK-M (GND)



PROJECT : R13
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PCH 6/6 (GND)	1A

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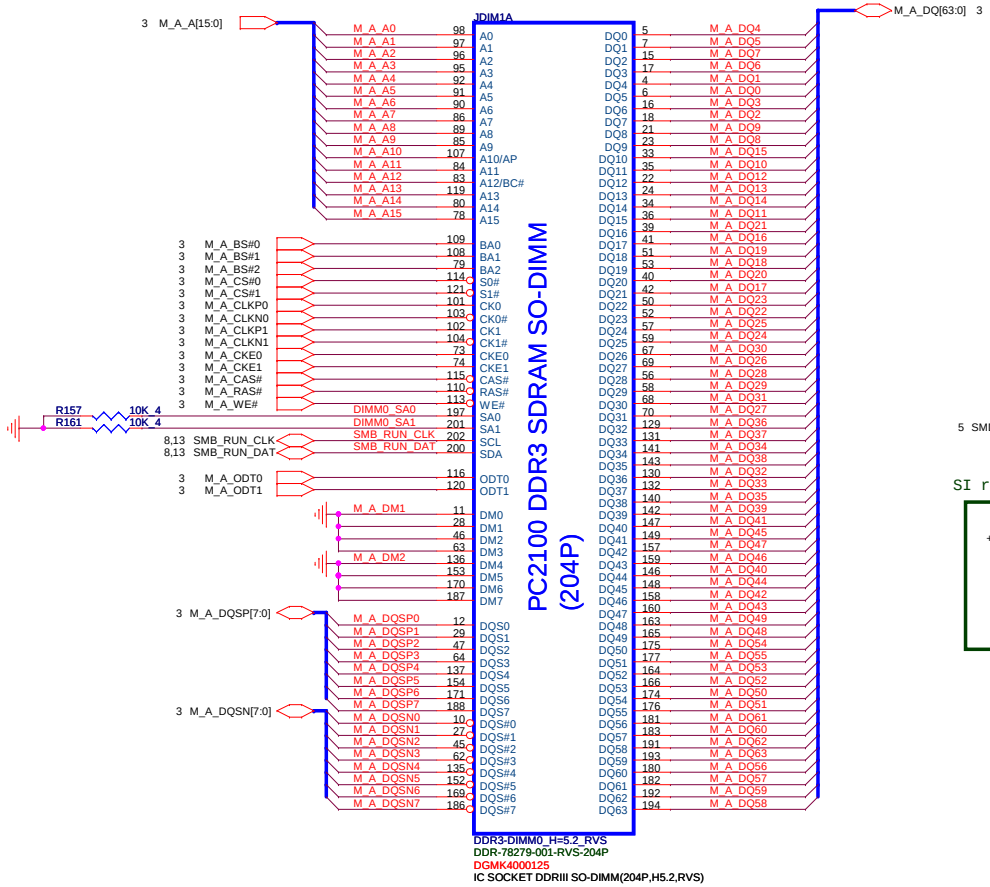
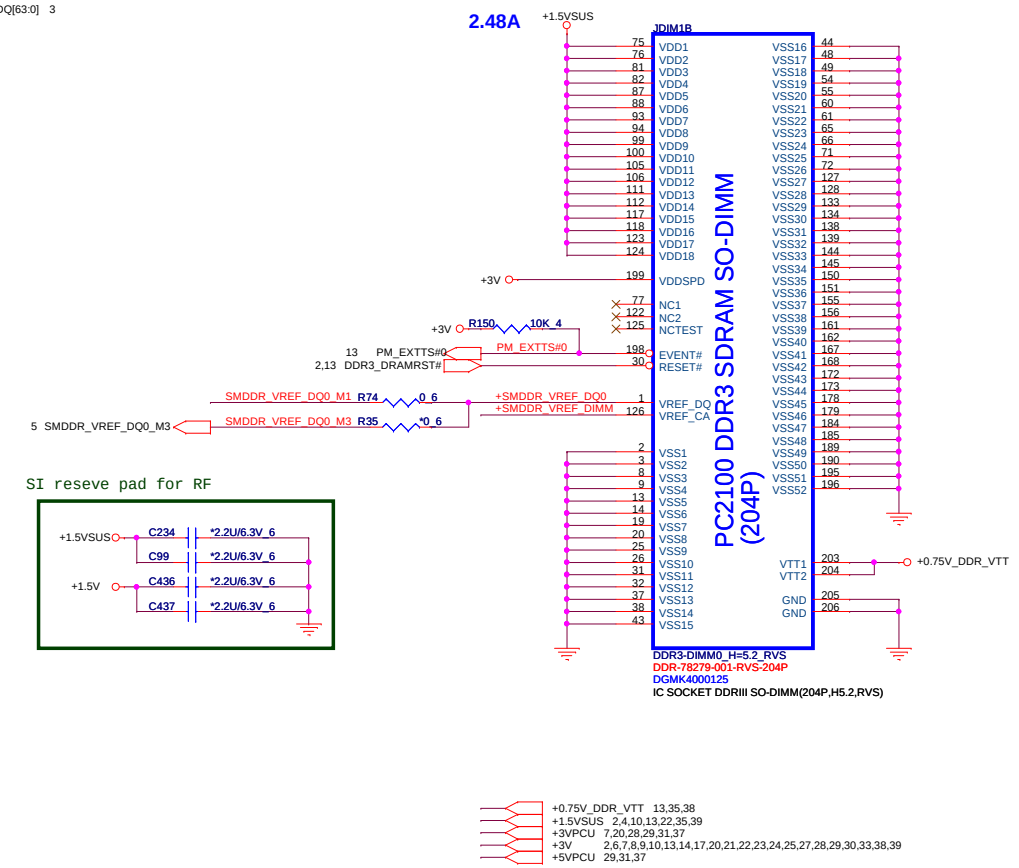


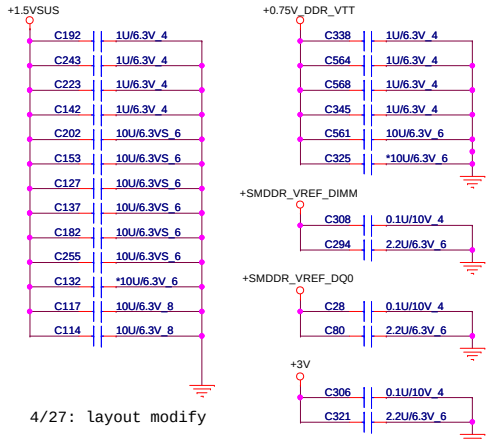


SI reseve pad for RF

VREF DQ0 M2 Solution

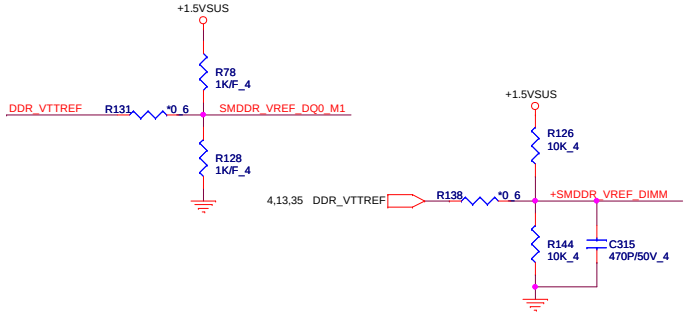
del M2 solution

Place these Caps near So-Dimm0.



4/27: layout modify

VREF DQ0 M1 Solution



PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM0-RVS (5.2H)	1A

NB5

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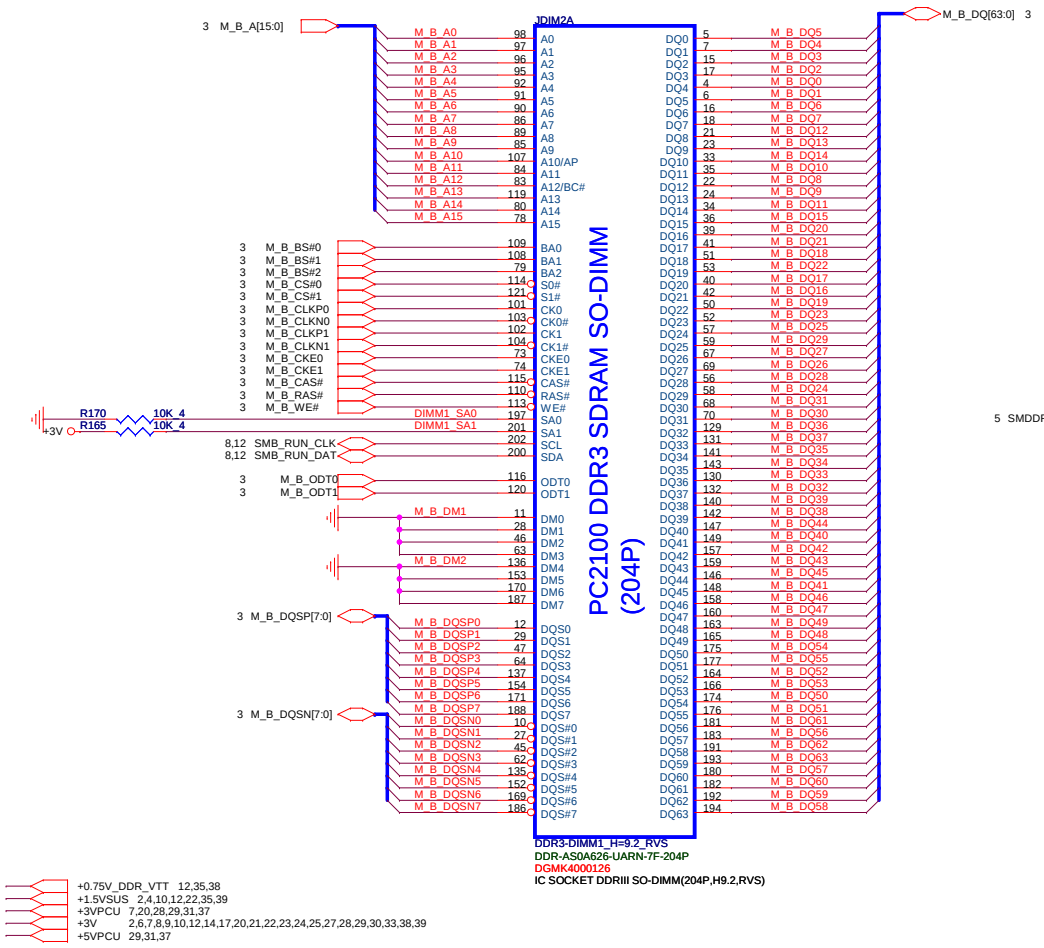
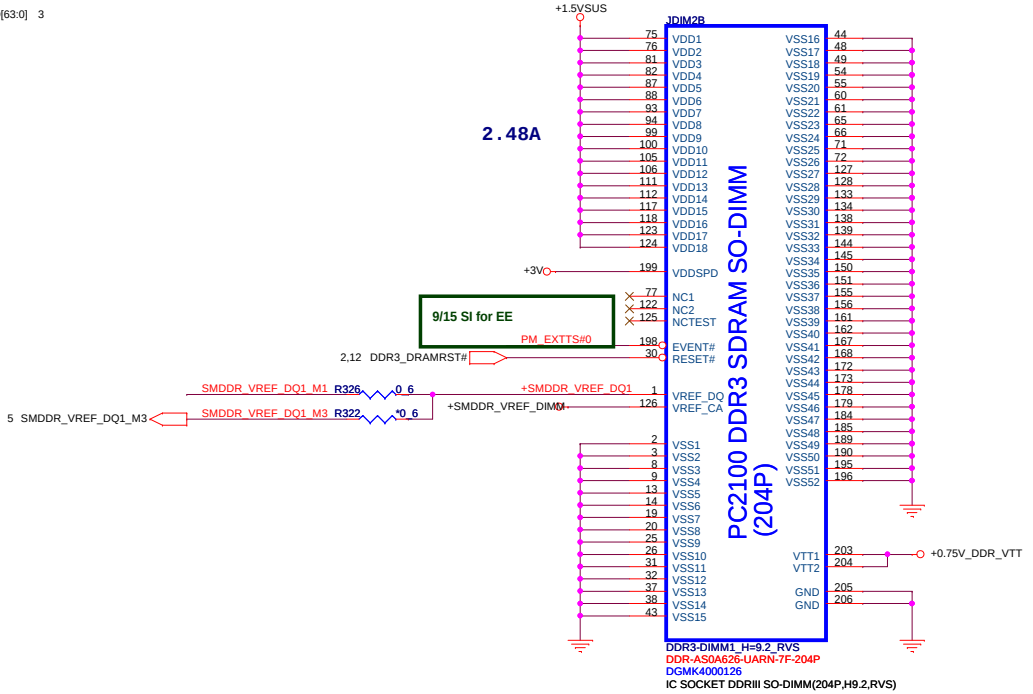
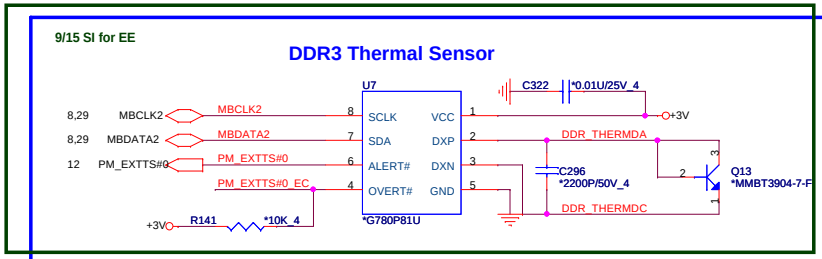


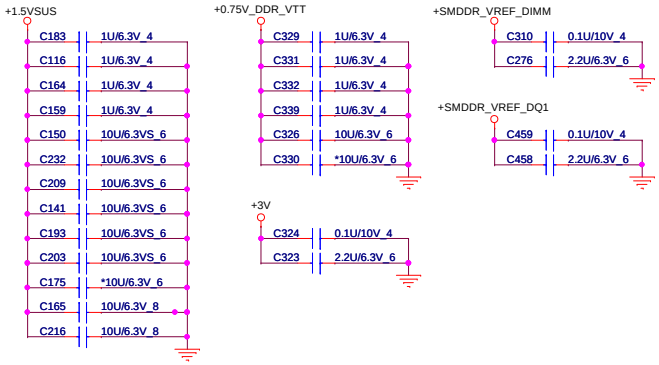




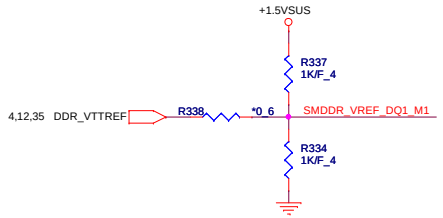
+0.75V_DDR_VTT 12,35,38
+1.5VSUS 2,4,10,12,22,35,39
+3VPCU 7,20,28,29,31,37
+3V 2,6,7,8,9,10,12,14,17,20,21,22,23,24,25,27,28,29,30,33,38,39
+5VPCU 29,31,37

del M2 solution

Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution



PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM1-RVS (9.2H)	1A

NB5

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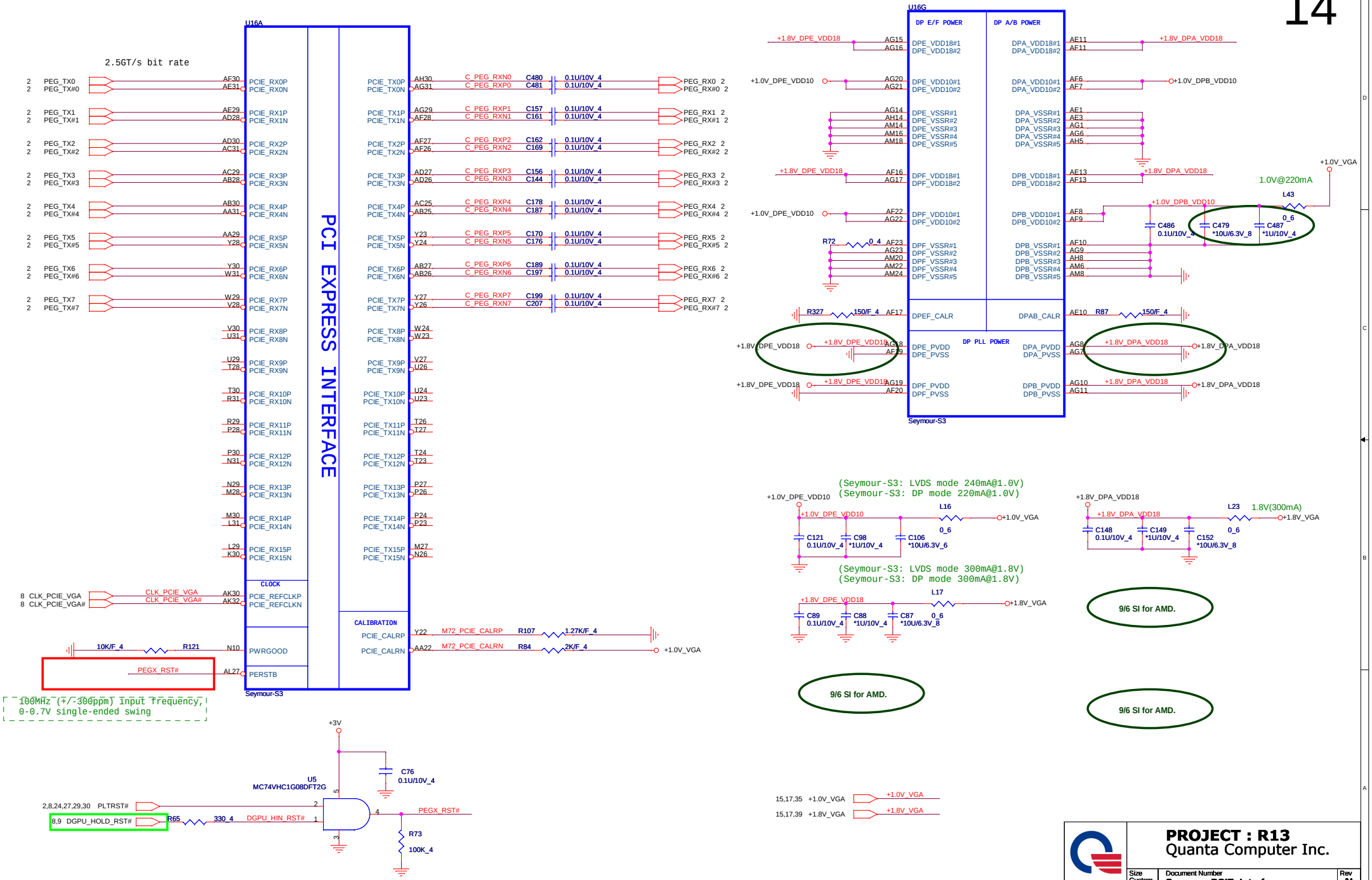

NB5

PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Seymour PCIE_Interface	1A

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MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Samsung- E die	64*16-800MHZ	K4W1G1646E-HC12
0001	Hynix- Vega die	64*16-800MHZ	H5TQ1G63DFR-12C
0010	Hynix- Vega die	128*16-800MHZ	H5TQ2G63BFR-12C
0011	Samsung- C die	128*16-800MHZ	K4W2G1646C-HC12
0100	Micron	128*16-800MHZ	MT41J128M16HA-125:D
0101			Reserved
0110	Hynix- Vega die	64*16-900MHZ	H5TQ1G63DFR-11C
0111	Samsung- E die	64*16-900MHZ	K4W1G1646E-HC11
1000	Samsung- G die	64*16-900MHZ	K4W1G1646G-BC11
1001			Reserved
1010	Hynix- Vega die	128*16-900MHZ	H5TQ2G63BFR-11C
1011	Samsung- C die	128*16-900MHZ	K4W2G1646C-HC11
1100			Reserved
1101			Reserved
1110			Reserved
1111			Reserved

GPIO15 GPIO20

Seymour	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	1V
H	1	0	1.1V (Default)
TBD	1	1	NA

Access to SCL and SDA is mandatory on BACO designs for debug purposes

GPIO22(ROMCS#) PD without external VBIOS ROM

If no contact this pin to LVDS need pull low

Seymour uninstall Ra to meet AF24 N/C

DAC2 is NC on Seymour

Reserve for DB debug only

Reserve for DB debug only

Seymour-S3--NC ROBSON--install

For Int Clk 27Mhz

9/3 SI for H/W.

Robson-- Install Seymour- NC BACO mode -- install

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PROJECT : R13
Quanta Computer Inc.
NB5
Size: Custom | Document Number: Seymour Main | Rev: 3A
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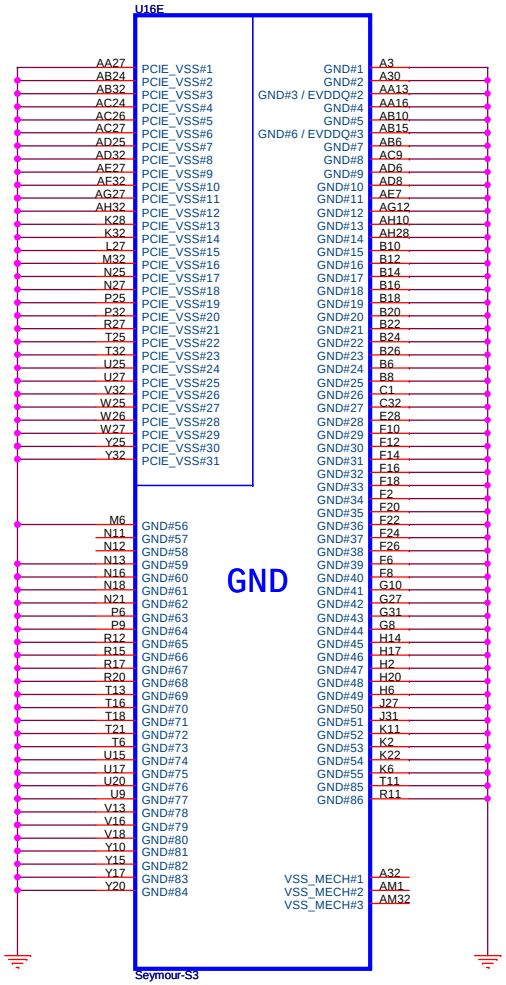
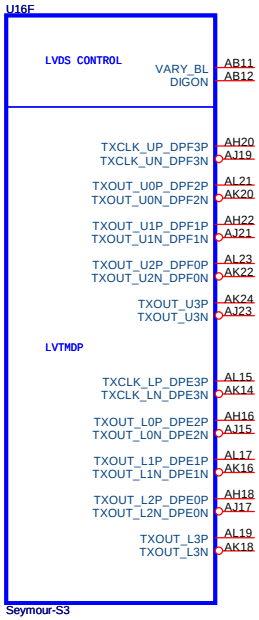
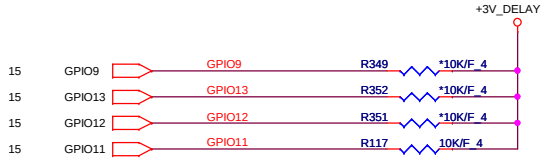






CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

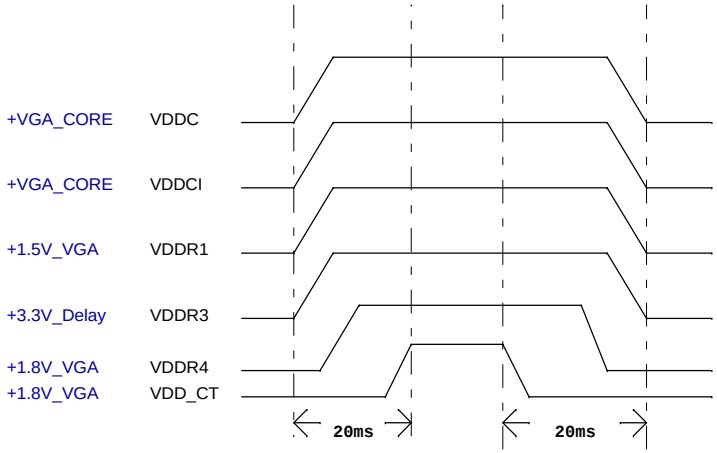
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

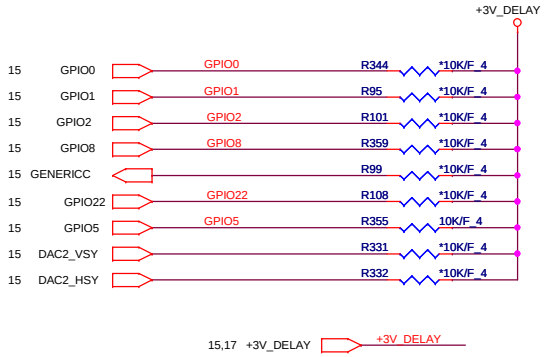
Power Up/Down Sequence



Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Seymour GND / LVDS/ Straps	3A
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PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%

6,7,10,21,22,23,25,28,30,38 +5V
2,6,7,8,9,10,12,13,14,20,21,22,23,24,25,27,28,29,30,33,38,39 +3V
14,15,35 +1.0V_VGA
39 +3V_VGA
39 +VGA_CORE

+5V
+3V
+1.0V_VGA
+3V_VGA
+VGA_CORE

U16D

MEM I/O
LEVEL TRANSLATION
I/O
MEM CLK
PLL
BACK BIAS
PCIE
CORE
POWER
ISOLATED CORE I/O
Seymour-S3

+1.5V_VGA
1.5V (DDR3, MVDDQ = 1.5V@2.0A)
C580 1U/10V_4
C259 1U/10V_4
C290 1U/10V_4
C277 1U/10V_4
C293 1U/10V_4
C278 10U/6.3VS_6
C295 10U/6.3VS_6
C275 10U/6.3VS_6

1.8V(110mA VDD_CT)
+1.8V_VGA
L15 PBY160808T-121Y-N(120,2.5A)
+1.8V_VDD_CT
C104 10U/6.3VS_6
C115 1U/10V_4
C196 1U/10V_4
C124 1U/10V_4
C205 0.1U/10V_4

Gated 3.3V
60mA by
VDDC

+3V_VGA
L18 0_6
+3V_DELAY
C188 1U/10V_4
C198 1U/10V_4
C185 1U/10V_4
C103 10U/6.3VS_6

VDD_R3 --IO power for
3.3 V pins (e.g.
GPIO's). 3.3 V ± 5%

1.8V(75mA MPV18)
BLM18PG471SN1D(470,1000MA)
+1.8V_VGA
L29
MPV18
C302 1U/10V_4
C304 0.1U/10V_4

+VDDR4
+1.8V_VGA
L24
PBY160808T-121Y-N(120,2.5A)
1.8V(170mA VDDR4)
C168 10U/6.3VS_6
C171 1U/10V_4
C208 0.1U/10V_4
T11

1.8V(90mA SPV18)
+1.8V_VGA
L28 PBY160808T-121Y-N(120,2.5A) SPV18
C291 1U/10V_4
C292 0.1U/10V_4

+1.8V_PCIE_VDDR
AM30 PCIE_PVDD
MPV18 L8 MPV18
SPV18 H7 SPV18
H8 SPV10
J7 SPVSS

1.0V_VGA(100mA SPV10)
BLM18PG471SN1D(470,1000MA)
+1.0V_VGA
L46
+1.0V_VGA_SPV10
C537 10U/6.3VS_6
C279 0.1U/10V_4
C543 1U/10V_4

L17 VDDRHA
L16 VSSRHA
M11 BBP#1
M12 BBP#2

PCIE_VDDR#1 AB23
PCIE_VDDR#2 AC23
PCIE_VDDR#3 AD24
PCIE_VDDR#4 AE24
PCIE_VDDR#5 AE25
PCIE_VDDR#6 AE26
PCIE_VDDR#7 AF25
PCIE_VDDR#8 AG26

PCIE_VDDC#1 L23
PCIE_VDDC#2 L24
PCIE_VDDC#3 L25
PCIE_VDDC#4 L26
PCIE_VDDC#5 M22
PCIE_VDDC#6 N22
PCIE_VDDC#7 N23
PCIE_VDDC#8 N24
PCIE_VDDC#9 R22
PCIE_VDDC#10 T22
PCIE_VDDC#11 U22
PCIE_VDDC#12 V22

VDDC#1 AA15
VDDC#2 N15
VDDC#3 N17
VDDC#4 R13
VDDC#5 R16
VDDC#6 R18
VDDC#7 Y21
VDDC#8 T12
VDDC#9 T15
VDDC#10 T17
VDDC#11 T20
VDDC#12 U13
VDDC#13 U16
VDDC#14 U18
VDDC#15 V21
VDDC#16 V15
VDDC#17 V17
VDDC#18 V20
VDDC#20 Y13
VDDC#21 Y16
VDDC#22 Y18
VDDC#23 /BIF_VDDC R21
VDDC#19/BIF_VDDC U21

VDDC#1 M13
VDDC#2 M15
VDDC#3 M16
VDDC#4 M17
VDDC#5 M18
VDDC#6 M20
VDDC#7 M21
VDDC#8 N20

VDDR3#1 AA17
VDDR3#2 AA18
VDDR3#3 AB17
VDDR3#4 AB18

VDDR4#1 / VDDR5 V12
VDDR4#2 Y12
VDDR4#3 / VDDR5 U12
NC#1 / VDDR4 AA11
DVCLK / VDDR4 Y11
NC#3 / VDDR5 V11
NC / VDDR5 U11

VDD_CT#1 AA20
VDD_CT#2 AA21
VDD_CT#3 AB20
VDD_CT#4 AB21

VDDR1#1 H13
VDDR1#2 H16
VDDR1#3 H19
VDDR1#4 J10
VDDR1#5 J23
VDDR1#6 J24
VDDR1#7 J9
VDDR1#8 K10
VDDR1#9 K23
VDDR1#10 K24
VDDR1#11 K9
VDDR1#12 L11
VDDR1#13 L12
VDDR1#14 L13
VDDR1#15 L20
VDDR1#16 L21
VDDR1#17 L22

+1.8V_PCIE_VDDR
1.8V(500mA)
PBY160808T-221Y-N(220,2A)
L19
+1.8V_VGA
C191 0.1U/10V_4
C125 0.1U/10V_4
C131 1U/10V_4
C109 1U/10V_4
C108 1U/10V_4
C179 1U/10V_4
C110 1U/10V_4
C139 10U/6.3VS_6

+1.0V_VGA
+1.0V_PCIE_VDDC
1.0V(2.0A)
+1.0V_PCIE_VDDC
L26 0_8
C245 1U/10V_4
C235 1U/10V_4
C241 1U/10V_4
C221 1U/10V_4
C271 1U/10V_4
C273 1U/10V_4
C257 1U/10V_4
C231 10U/6.3VS_6

VDDC+VDDCI
0.85~1.1V(15A peak)(Ripple < 87.2mV)
+VGA_CORE
C250 1U/10V_4
C247 1U/10V_4
C249 1U/10V_4
C246 1U/10V_4
C228 1U/10V_4
C212 1U/10V_4
C211 1U/10V_4
C460 10U/6.3VS_6
C230 1U/10V_4
C225 2.2U/6.3V_4
C233 1U/10V_4
C258 10U/6.3V_8
C224 1U/10V_4
C204 1U/10V_4
C206 1U/10V_4
C201 1U/10V_4
C217 2.2U/6.3V_4
C210 1U/10V_4
C186 1U/10V_4
C118 1U/10V_4
C195 1U/10V_4
C70 10U/6.3VS_6
C68 10U/6.3VS_6
C119 10U/6.3VS_6
C462 10U/6.3VS_6
C461 10U/6.3VS_6
C71 10U/6.3VS_6

Note1.
BIF_VDDC R114 *0_4 +VGA_CORE
Ra

0.95V~1.1V(2A VDDCI)
+VDDCI
L25 0_8
+VGA_CORE
C267 1U/10V_4
C253 1U/10V_4
C248 1U/10V_4
C218 10U/6.3VS_6
C219 10U/6.3VS_6
C262 10U/6.3VS_6

39 PX_MODE1
Q45
PX_EN
2N7002
9/9 SI for AMD
PX_MODE R783 *0_4 PX_MODE1

Support BACO Mode

+3V
R372 *10K_4
39 PX_MODE
R369 0_4
18 PX_EN
Q33 2N7002
R376 5.1K/F_4
9/9 SI for AMD
6,29 EC_PWROK

+3V
R366 100K/F_4
Q28 2N7002
Q31 2N7002
8,9,29,35,39 DGPU_PWROK

+3V
C534 0.1U/10V_4
PX_MODE
U17 TC7SH08FU
BACO_EN

+5V
R383 1K_4
R380 1K_4
PX_EN##
PX_EN#
Q30 2N7002
Q32 2N7002

+1.0V_VGA
Q15 AO3416
Q27 AO3416
PX_EN#
Q14 AO3416
Q29 AO3416
+VGA_CORE
PX_EN##
BIF_VDDC
C287 22U/6.3VS_8
C251 10U/6.3V_6
C266 10U/6.3V_6
C229 2.2U/6.3V_4
C213 2.2U/6.3V_4

Note1. 1. No BACO Support :BIF_VDDC shorts with VDDC (Install Ra)

2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is Support. (Uninstall Ra)

PX_EN = 0, for Normal Operation
PX_EN = 1, for BACO MODE

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PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Seymour_Power_and_NC	1A

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U16C

MEMORY INTERFACE

Seymour-S3

VMA_DQ0	K27	DQA_0	
VMA_DQ1	J29	DQA_1	
VMA_DQ2	H30	DQA_2	
VMA_DQ3	H32	DQA_3	
VMA_DQ4	G29	DQA_4	
VMA_DQ5	F28	DQA_5	
VMA_DQ6	F32	DQA_6	
VMA_DQ7	F30	DQA_7	
VMA_DQ8	C30	DQA_8	
VMA_DQ9	F27	DQA_9	
VMA_DQ10	A28	DQA_10	
VMA_DQ11	C28	DQA_11	
VMA_DQ12	E27	DQA_12	
VMA_DQ13	G26	DQA_13	
VMA_DQ14	D26	DQA_14	
VMA_DQ15	F25	DQA_15	
VMA_DQ16	A25	DQA_16	
VMA_DQ17	C25	DQA_17	
VMA_DQ18	E25	DQA_18	
VMA_DQ19	D24	DQA_19	
VMA_DQ20	E23	DQA_20	
VMA_DQ21	F23	DQA_21	
VMA_DQ22	D22	DQA_22	
VMA_DQ23	F21	DQA_23	
VMA_DQ24	E21	DQA_24	
VMA_DQ25	D20	DQA_25	
VMA_DQ26	F19	DQA_26	
VMA_DQ27	A19	DQA_27	
VMA_DQ28	D18	DQA_28	
VMA_DQ29	F17	DQA_29	
VMA_DQ30	A17	DQA_30	
VMA_DQ31	C17	DQA_31	
VMA_DQ32	E17	DQA_32	
VMA_DQ33	D16	DQA_33	
VMA_DQ34	E15	DQA_34	
VMA_DQ35	A15	DQA_35	
VMA_DQ36	D14	DQA_36	
VMA_DQ37	F13	DQA_37	
VMA_DQ38	A13	DQA_38	
VMA_DQ39	C13	DQA_39	
VMA_DQ40	E11	DQA_40	
VMA_DQ41	A11	DQA_41	
VMA_DQ42	C11	DQA_42	
VMA_DQ43	F11	DQA_43	
VMA_DQ44	A9	DQA_44	
VMA_DQ45	C9	DQA_45	
VMA_DQ46	F9	DQA_46	
VMA_DQ47	D8	DQA_47	
VMA_DQ48	E7	DQA_48	
VMA_DQ49	A7	DQA_49	
VMA_DQ50	C7	DQA_50	
VMA_DQ51	F7	DQA_51	
VMA_DQ52	A5	DQA_52	
VMA_DQ53	E5	DQA_53	
VMA_DQ54	C3	DQA_54	
VMA_DQ55	E1	DQA_55	
VMA_DQ56	G7	DQA_56	
VMA_DQ57	G6	DQA_57	
VMA_DQ58	G1	DQA_58	
VMA_DQ59	G3	DQA_59	
VMA_DQ60	J6	DQA_60	
VMA_DQ61	J1	DQA_61	
VMA_DQ62	J3	DQA_62	
VMA_DQ63	J5	DQA_63	

MAA_0	K17	VMA_MA0	
MAA_1	J20	VMA_MA1	
MAA_2	H23	VMA_MA2	
MAA_3	G23	VMA_MA3	
MAA_4	G24	VMA_MA4	
MAA_5	H24	VMA_MA5	
MAA_6	J19	VMA_MA6	
MAA_7	K19	VMA_MA7	
MAA_8	J14	VMA_MA8	
MAA_9	K14	VMA_MA9	
MAA_10	J11	VMA_MA10	
MAA_11	J13	VMA_MA11	
MAA_12	H11	VMA_MA12	
MAA_13/BA2	G11	VMA_BA2	
MAA_14/BA0	J16	VMA_BA0	
MAA_15/BA1	L15	VMA_BA1	
DQMA_0	E32	VMA_DM0	
DQMA_1	E30	VMA_DM1	
DQMA_2	A21	VMA_DM2	
DQMA_3	C21	VMA_DM3	
DQMA_4	E13	VMA_DM4	
DQMA_5	D12	VMA_DM5	
DQMA_6	E3	VMA_DM6	
DQMA_7	F4	VMA_DM7	
RDQSA_0	H28	VMA_RDQS0	
RDQSA_1	C27	VMA_RDQS1	
RDQSA_2	A23	VMA_RDQS2	
RDQSA_3	E19	VMA_RDQS3	
RDQSA_4	E15	VMA_RDQS4	
RDQSA_5	D10	VMA_RDQS5	
RDQSA_6	D6	VMA_RDQS6	
RDQSA_7	G5	VMA_RDQS7	
WDQSA_0	H27	VMA_WDQS0	
WDQSA_1	A27	VMA_WDQS1	
WDQSA_2	C23	VMA_WDQS2	
WDQSA_3	C19	VMA_WDQS3	
WDQSA_4	C15	VMA_WDQS4	
WDQSA_5	E9	VMA_WDQS5	
WDQSA_6	C5	VMA_WDQS6	
WDQSA_7	H4	VMA_WDQS7	
ODTA0	L18	VMA_ODT0	
ODTA1	K16	VMA_ODT1	
CLKA0	H26	VMA_CLK0	
CLKA0B	H25	VMA_CLK0#	
CLKA1	G9	VMA_CLK1	
CLKA1B	H9	VMA_CLK1#	
RASA0B	G22	VMA_RAS0#	
RASA1B	G17	VMA_RAS1#	
CASA0B	G19	VMA_CAS0#	
CASA1B	G16	VMA_CAS1#	
CSA0B_0	H22	VMA_CS0#	
CSA0B_1	J22		
CSA1B_0	G13	VMA_CS1#	
CSA1B_1	K13		
CKEA0	K20	VMA_CKE0	
CKEA1	J17	VMA_CKE1	
WEA0B	G25	VMA_WE0#	
WEA1B	H10	VMA_WE1#	
PX_EN	AB16	PX_EN	PX_EN 17
RSVD#2	G14		
RSVD#3	G20	VMA_MA13	
MVREFDA	K26		
MVREFSA	J26		
MEM_CALRN0	J25		
NC/TESTEN#2	K7		
MEM_CALRP1/DPC_CALR	J8		
MEM_CALRP0	K25		
DRAM_RST	L10		
CLKTESTA	K8		
CLKTESTB	L7		

19 VMA_ODT0 — VMA_ODT0
19 VMA_ODT1 — VMA_ODT1
19 VMA_RAS0# — VMA_RAS0#
19 VMA_RAS1# — VMA_RAS1#
19 VMA_CAS0# — VMA_CAS0#
19 VMA_CAS1# — VMA_CAS1#
19 VMA_WE0# — VMA_WE0#
19 VMA_WE1# — VMA_WE1#
19 VMA_CS0# — VMA_CS0#
19 VMA_CS1# — VMA_CS1#
19 VMA_CKE0 — VMA_CKE0
19 VMA_CKE1 — VMA_CKE1
19 VMA_CLK0 — VMA_CLK0
19 VMA_CLK0# — VMA_CLK0#
19 VMA_CLK1 — VMA_CLK1
19 VMA_CLK1# — VMA_CLK1#
19 VMA_WDQS[7..0] — VMA_WDQS[7..0]
19 VMA_RDQS[7..0] — VMA_RDQS[7..0]
19 VMA_DM[7..0] — VMA_DM[7..0]
19 VMA_DQ[63..0] — VMA_DQ[63..0]
19 VMA_MA[13..0] — VMA_MA[13..0]
19 VMA_BA0 — VMA_BA0
19 VMA_BA1 — VMA_BA1
19 VMA_BA2 — VMA_BA2

support 1Gbit VRAM (64M X 16)

DIVIDER RESISTORS	GDDR5	DDR3
MVREF TO 1.8V (Ra)	40.2R	40.2R
MVREF TO GND (Rb)	100R	100R

PLACE MVREFD DIVIDERS
AND CAPS CLOSE TO ASIC

+1.5V_VGA
R425 Ra 40.2/F_4
MVREFD
C570 0.1U/10V_4
R421 Rb 100/F_4
+1.5V_VGA
R431 Ra 40.2/F_4
MVREFS
C583 0.1U/10V_4
R429 Rb 100/F_4

+1.5V_VGA
R415 243/F_4
R133 3.1K/F_4
R132 150/F_4
R416 243/F_4
DRAM_RST

C261 *0.1U/10V_4
C514 *0.1U/10V_4
R129 *51.1/F_4
R353 *51.1/F_4

route 50ohms
single-ended/100ohms diff
and keep short
Debug only, for clock observation,
if not needed, DNI

17,19,22,39 +1.5V_VGA — +1.5V_VGA

DRAM_RST — R171 10_4 — R177 51/F_4 — DRAM_RST_M — DRAM_RST_M 19
R174 5.1K/F_4
C335 120P/50V_4
9/3 SI for H/W.

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PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Seymour/MEM_Interface	1A

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512MB DDR3

18 VMA_MA[13..0]
18 VMA_DM[7..0]
VMA_MA[13..0]
18 VMA_DQ[63..0]
18 VMA_WDQS[7..0]
18 VMA_RDQS[7..0]

U10 / U19 / U9 / U20 — K4W1G1646E-HC12 (100-BALL SDRAM DDR3)

Should be 243 Ohms +-1%
R187 243/F_4
R414 243/F_4
R166 243/F_4
R413 243/F_4

+1.5V_VGA

R428 4.99K/F_4
R424 4.99K/F_4
C573 0.1U/10V_4
R160 4.99K/F_4
R162 4.99K/F_4
C328 0.1U/10V_4
R418 4.99K/F_4
R426 4.99K/F_4
C574 0.1U/10V_4
R180 4.99K/F_4
R176 4.99K/F_4
C342 0.1U/10V_4
R183 4.99K/F_4
R179 4.99K/F_4
C348 0.1U/10V_4
R175 4.99K/F_4
R178 4.99K/F_4
C340 0.1U/10V_4
R417 4.99K/F_4
R419 4.99K/F_4
C566 0.1U/10V_4
R410 4.99K/F_4
R412 4.99K/F_4
C562 0.1U/10V_4

VMA_CLK0
R182 56.2/F_4
VMA_CLK0_COMM
C357 0.01U/16V_4
R184 56.2/F_4
VMA_CLK0#
VMA_CLK1
R167 56.2/F_4
VMA_CLK1_COMM
C333 0.01U/16V_4
R172 56.2/F_4
VMA_CLK1#

C565 C362 C361 C360 C359 C567 C569 C349 1U/6.3V_4
C571 C572 C577 C350 C354 C347 C581 C579 1U/6.3V_4
C586 C582 C356 C358 10U/6.3VS_6
C555 C551 C575 C316 C578 C320 C548 C546 0.1U/10V_4
C319 C585 C587 C317 C351 C318 C337 C343 0.1U/10V_4

	QCI PN
SAMSUNG	AKD5LGGT502
HYNIX	AKD5LZGTW00

NB5

PROJECT : R13
Quanta Computer Inc.

Size: Custom | Document Number: Seymour VRAM(DDR3 BGA96) | Rev: 3A
Date: Saturday, September 18, 2010 | Sheet 19 of 39

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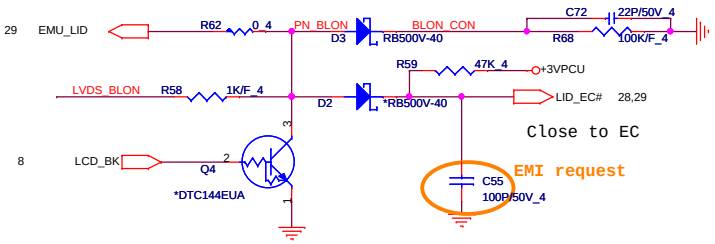
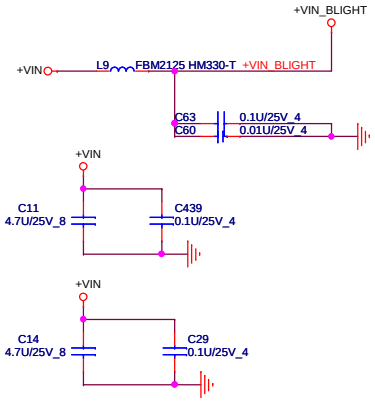
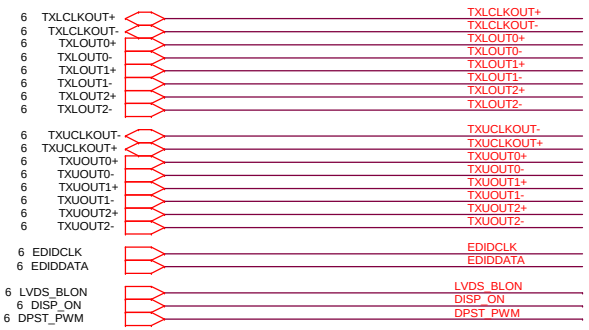
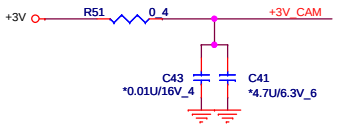
LID Switch



100mA

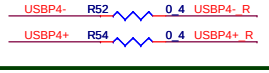




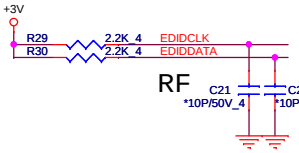


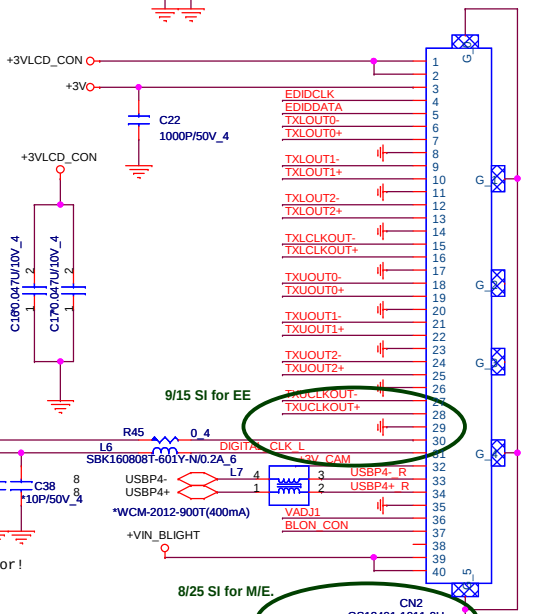
Please note that 2011 camera is +3V a We do not need to use 5V -> 3.95V regulator!

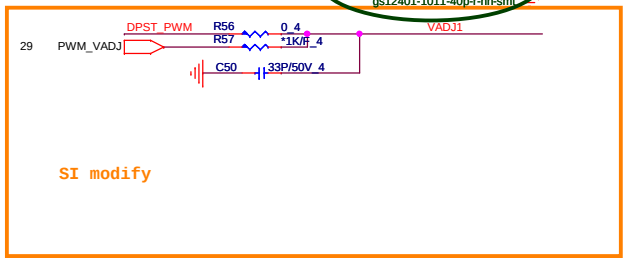
follow L7 location



RF SI change to AX type

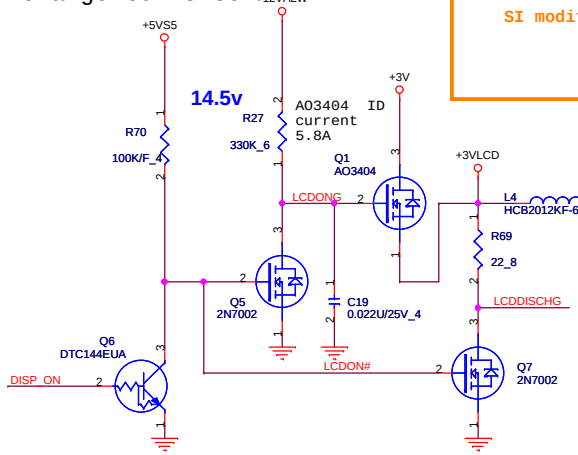






1A

change to +5VS5



2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,27,28,29,30,33,38,39 +3V
7,28,29,31,37 +3VPCU
6,7,10,17,21,22,23,25,28,30,38 +5V
23,37,38,39 +12VALW
31,32,34,35,36,37,38,39 +VIN

NB5

PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A

Date: Saturday, September 18, 2010 Sheet 20 of 39

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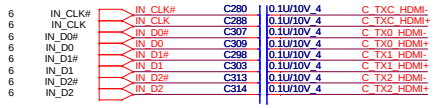
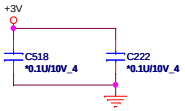
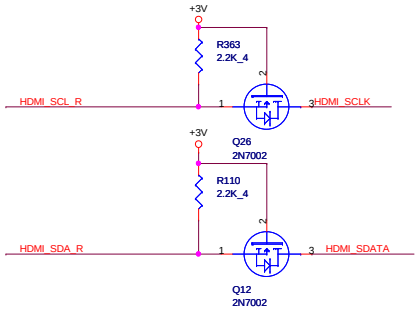
close to HDMI conn



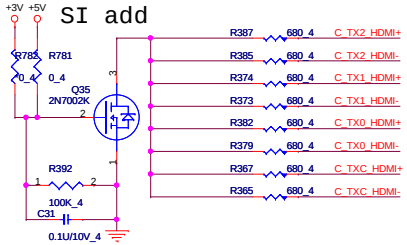


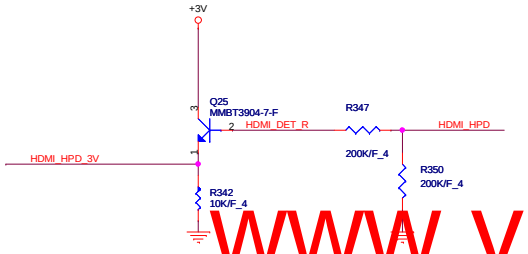
DISCRETE HDMI I2C SELECT

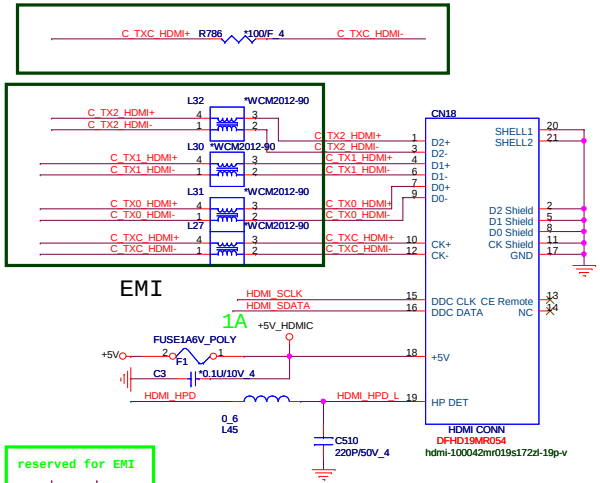
Close to HDMI Connector



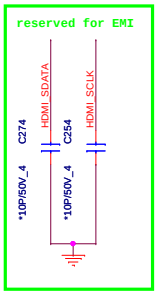
SI add

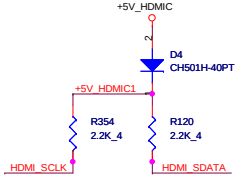






EMI





PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI CONN	3A

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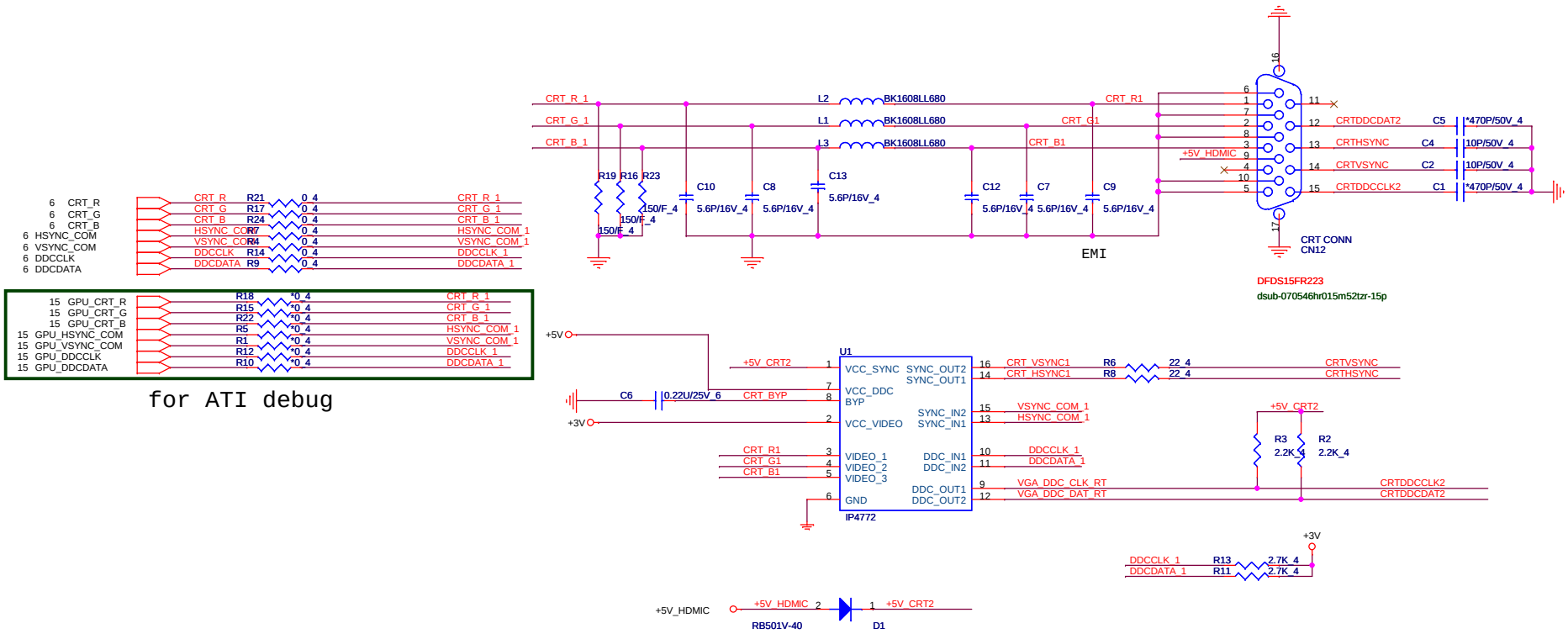
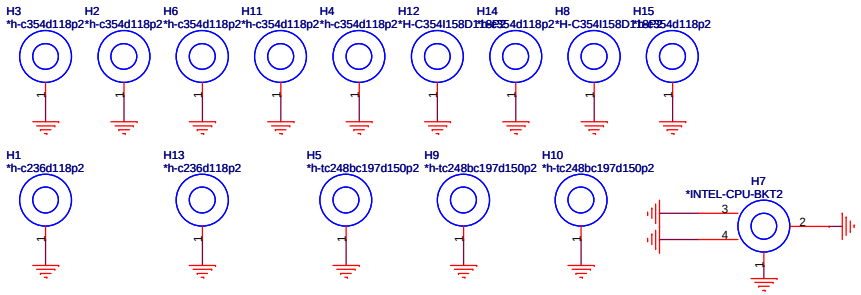
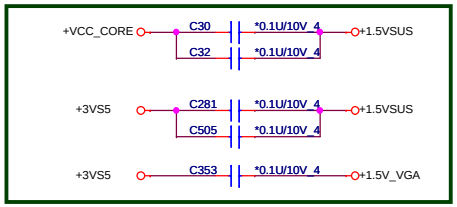
CRT PORT



HOLE





RF solution

NB5	PROJECT : R13 Quanta Computer Inc.	
Size: Custom	Document Number: CRT,Hole	Rev: 1A
Date: Saturday, September 18, 2010	Sheet 22 of 39	

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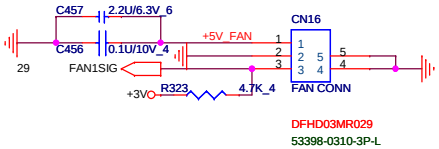
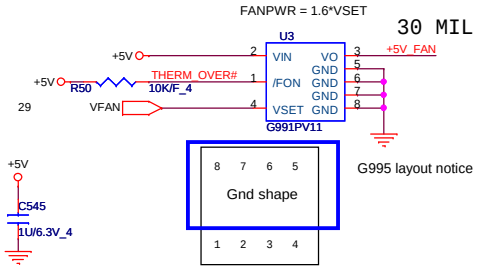
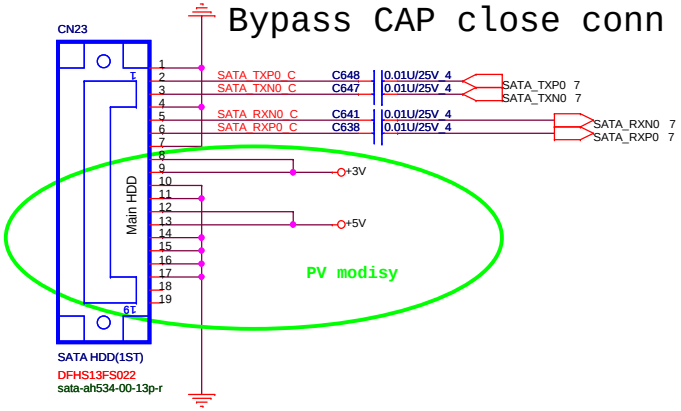
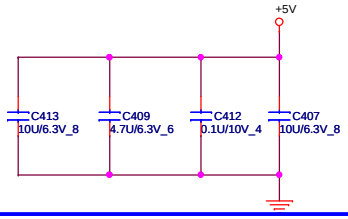
CPU FAN



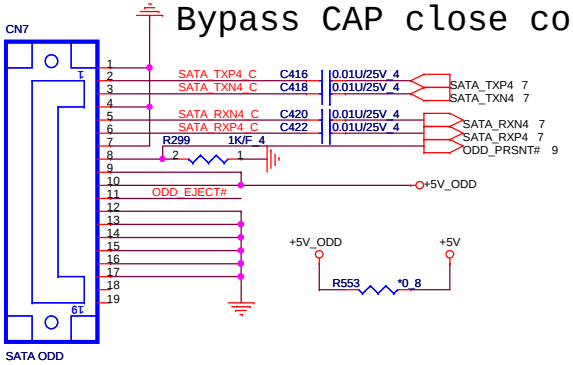


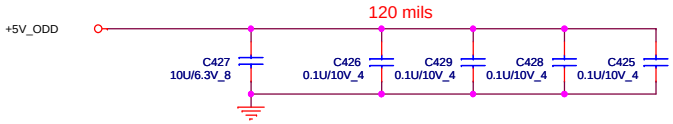
SATA HDD CONNECTOR



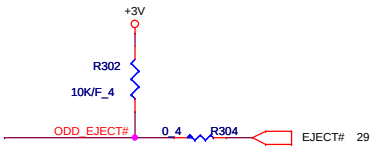


SATA ODD CONNECTOR

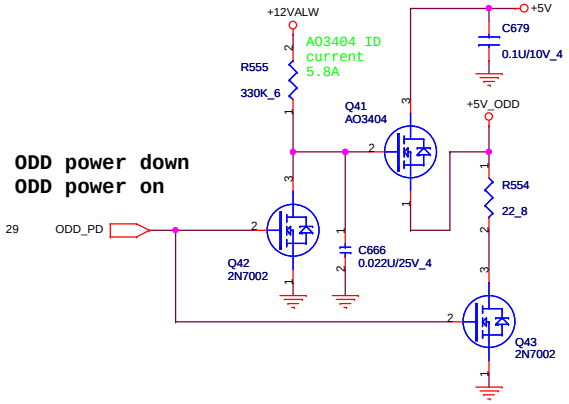




follow INTEL DG change eject PU to +3V.



High : ODD power down
Low : ODD power on



NB5	PROJECT : R13 Quanta Computer Inc.	
Size: Custom	Document Number: HDD/ODD/FAN	Rev: 1A
Date: Saturday, September 18, 2010	Sheet 23 of 39	

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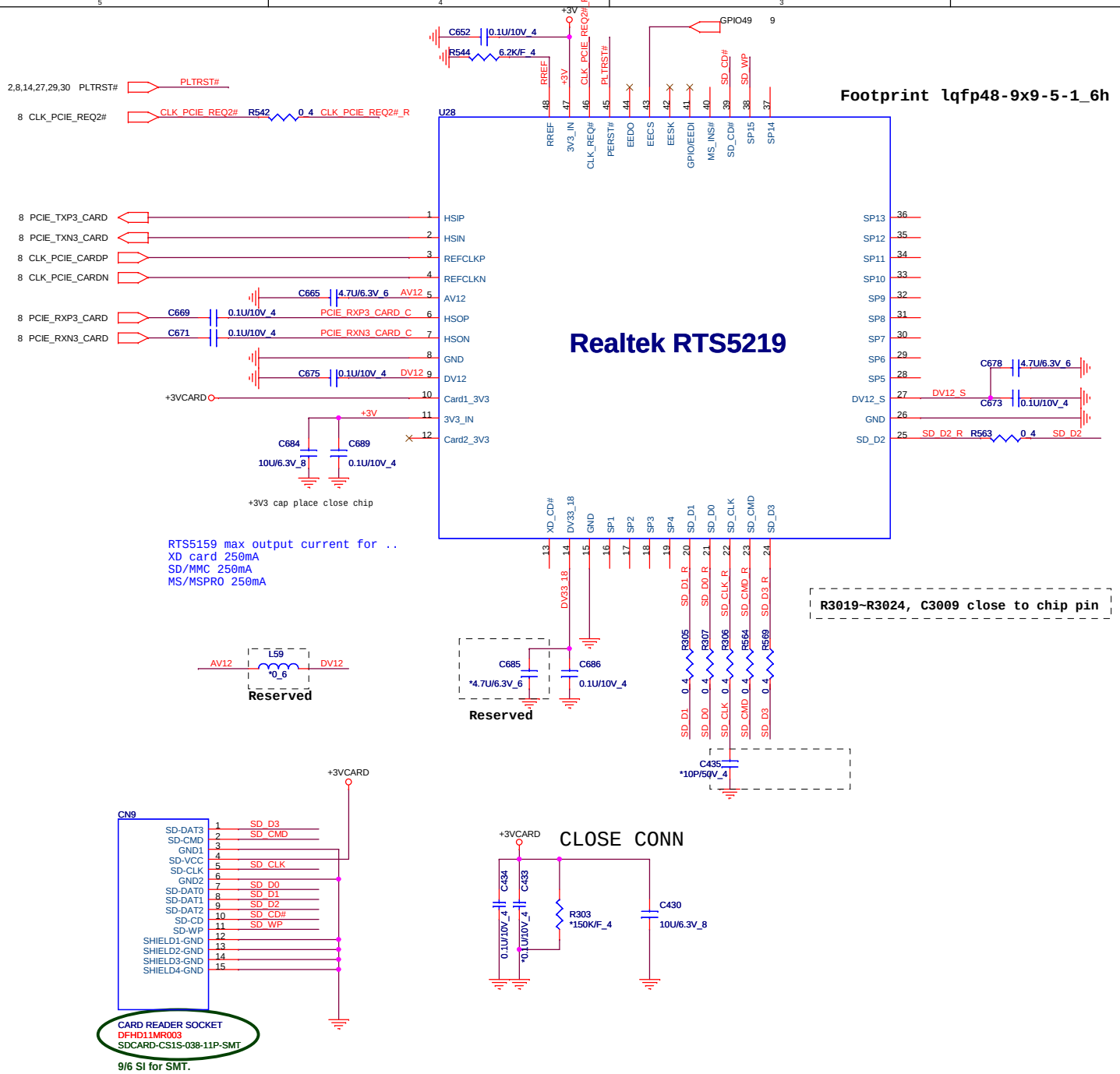

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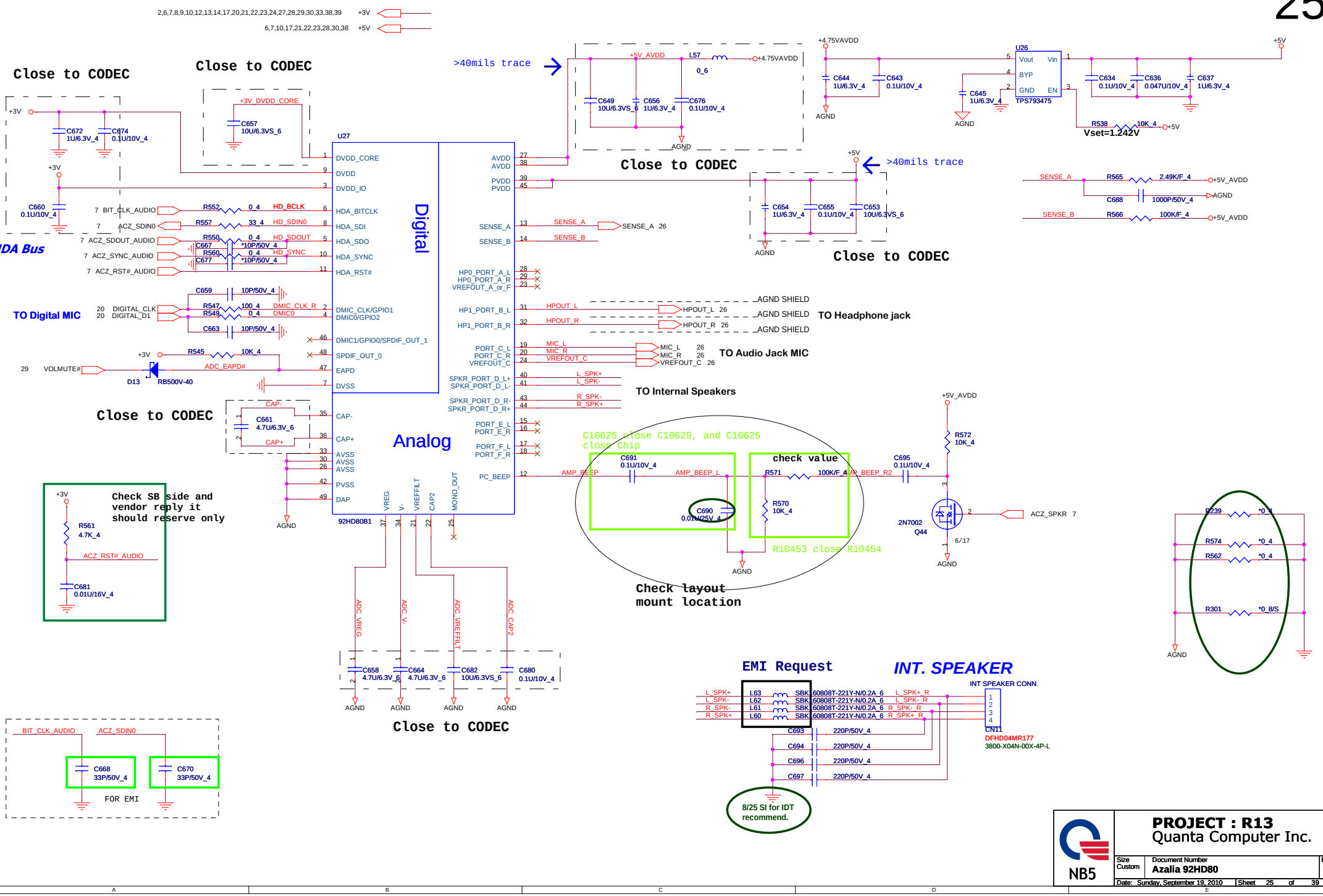
NB5	PROJECT : R13 Quanta Computer Inc.	
Size: Custom	Document Number: RTS5219 & CR SOCKET &HOLE	Rev: 3A
Date: Saturday, September 18, 2010	Sheet 24 of 39	



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BLUETOOTH

EMI request

BLUELED C423 *1000P/50V_4

300mA

change to +3VS5

+3VS5 +3VS5

R300 4.7K_4

Q22 ME2303T1

24mil 300mA

+3VPCU_BT

Q23 DTC144EUA

9,30 BT_OFF#

C424 *0.01U/16V_4

C417 0.1U/10V_4

C421 *10U/6.3V_8

CN8

BTCON_P1 T23

USBP2- BLUELED 29,30

USBP2+ USBP2- 8

+3VPCU_BT USBP2+ 8

C419 *1000P/50V_4

BLUE TOOTH CONN

87213-0600-6P-L

DFHD06MR058

LEFT SIDE USBX2

change to AL000547005

26

2A 2A

change to +5VS5

+5VS5 U23 80 mils (Iout=2A) +5V_USBP0

29 USBPW_ON#

C604 1U/6.3V_4

VIN1 VIN2 EN GND OUT3 OUT2 OUT1 OC

G547E2P81U

C591 470P/50V_4

C592 0.1U/10V_4

C588 470P/50V_4

C589 0.1U/10V_4

C584 100U/16V

change to ELEC CAP

1A

C334 *0.1U/10V_4

R168 0_4 L33 R173 0_4

*WCM2012-90

USBP0- USBP0+

+5V_USBP0 USBP0- R USBP0+ R

CN19 USB CONN

DFHD04MR133

usb-020173mr004s53qzl-4p-r-v

1A

C364 *0.1U/10V_4

R204 0_4 L36 R207 0_4

*WCM2012-90

USBP1- USBP1+

+5V_USBP0 USBP1- R USBP1+ R

CN20 USB CONN

DFHD04MR133

usb-020173mr004s53qzl-4p-r-v

Right SIDE USBX1

9/14 SI for HW

USBP8- R784 0_4 USBP8- R

USBP8+ R785 0_4 USBP8+ R

C26 0.1U/10V_4 +5VS5

SI del L5

CN1

29 USBPW_ON#

USBP8- USBP8+

L5 *WCM2012-90

USBP8- R USBP8+ R

USB board

DFFC06FR062

88513-0601-6P-L-SMT

10/21 change common mode choke to small board

EMI request

C20 220P/50V_4 USBPW_ON#

Line out

SENSE_PHONE R532 20K/F_4 SENSE_A

SENSE_MIC R272 10K/F_4 SENSE_A

SENSE_A 25

AGND SHIELD

AGND SHIELD

AGND SHIELD

25 HPOUT_L HPOUT_L R556 16/F_4 HPOUT_L1 L51 SBK160808T-301Y-N/0.2A_6 HPOUT_L2

25 HPOUT_R HPOUT_R R551 16/F_4 HPOUT_R1 L52 SBK160808T-301Y-N/0.2A_6 HPOUT_R2

R530 20K/F_4

R511 20K/F_4

C624 1000P/50V_4

C618 1000P/50V_4

AGND

C616 0.1U/10V_4 C619 0.1U/10V_4

AGND

CN22

DFTJ06FR335

audio-311105-2-6p

AEC_311105-2

Normal Open

AGND

SENSE_PHONE

MIC

25 VREFOUT_C VREFOUT_C C385 1U/6.3V_4 AGND

R264 3.9K/F_4

R255 3.9K/F_4

25 MIC_L MIC_L C650 2.2U/6.3V_6 MIC_L1 L37 SBK160808T-301Y-N/0.2A_6 MIC_IN_L

25 MIC_R MIC_R C651 2.2U/6.3V_6 MIC_R1 L38 SBK160808T-301Y-N/0.2A_6 MIC_IN_R

C391 220P/50V_4

C370 220P/50V_4

AGND

CN21

DFTJ06FR335

audio-311105-2-6p

AEC_311105-2

Normal Open

AGND AGND

SENSE_MIC

NB5

PROJECT : R13

Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB/BT/Audio JacK	1A

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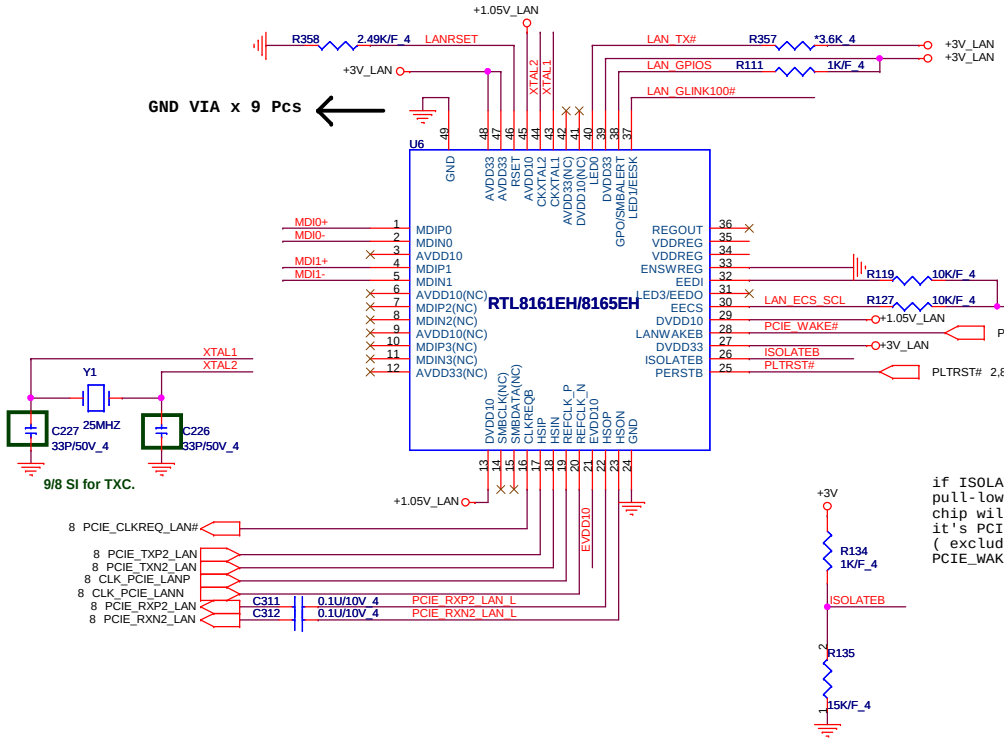
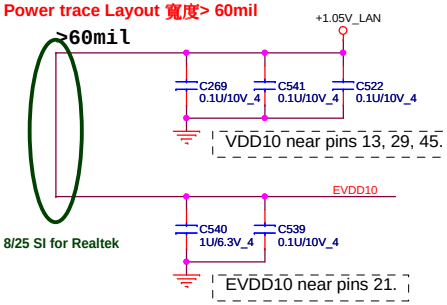


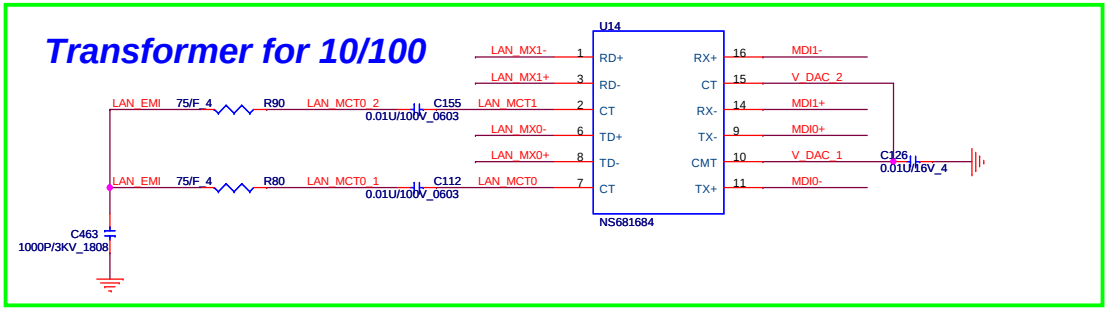
if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

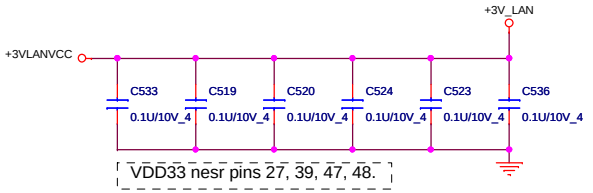
IND SMD 4.7UH +-20% 680MA(CBC2518T4R7M)
CV-4707MZ00

Power trace Layout 寬度> 60mil

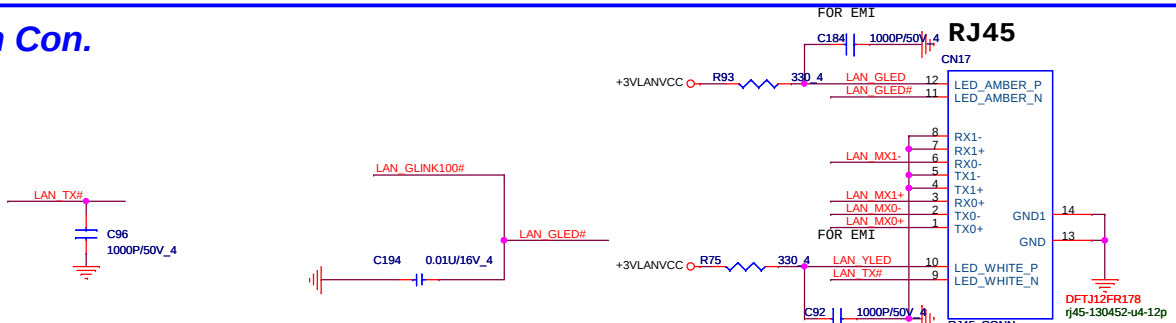


Transformer for 10/100





Lan Con.



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NB5

PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL8165EH	1A

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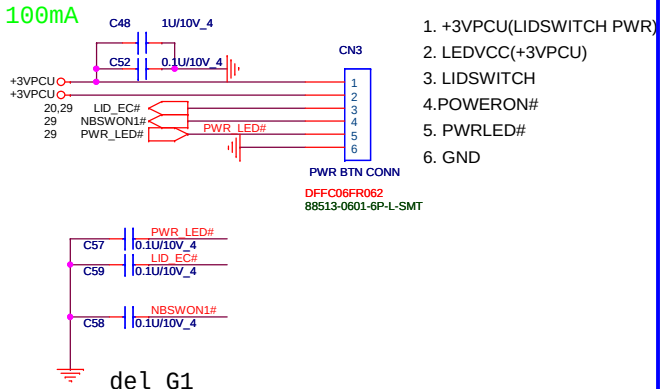
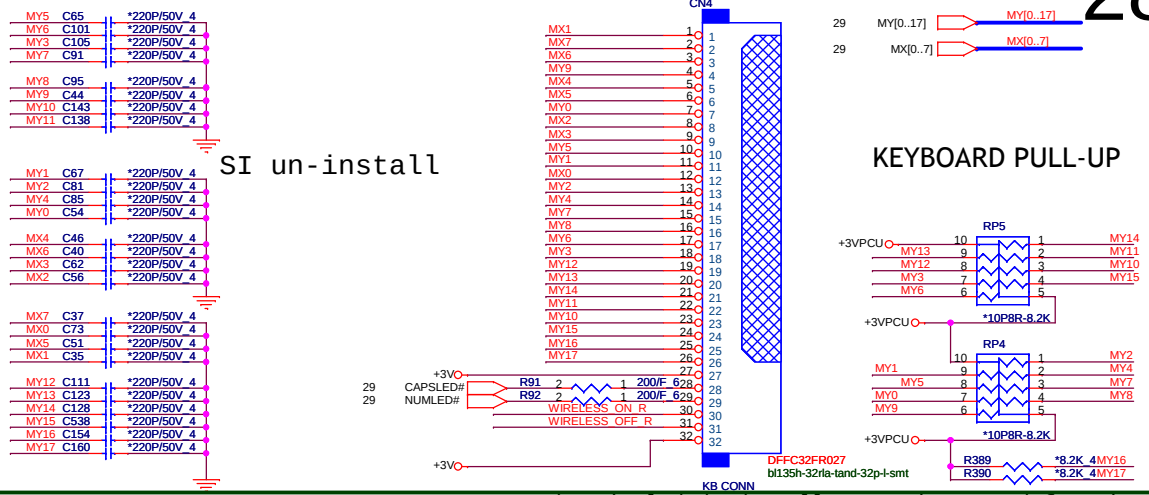
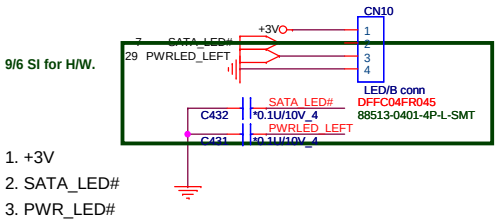
POWER BOTTON CONNECT

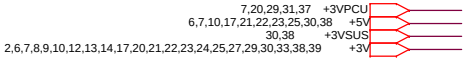


KEYBOARD Con.

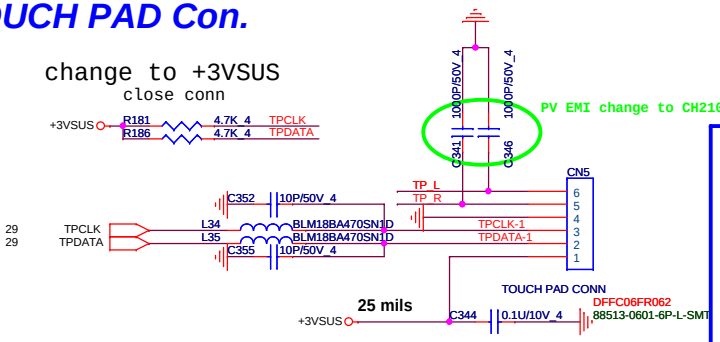


LED Con.

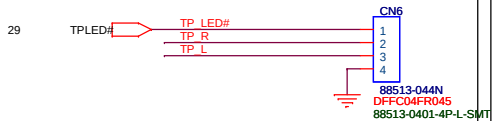




TOUCH PAD Con.



To TOUCH PAD SW board



NB5

PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/KB/SW/TP	1A

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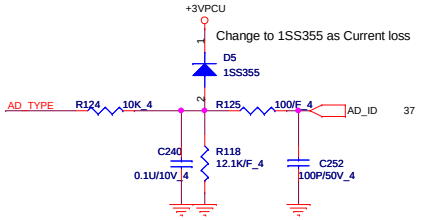
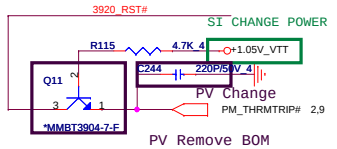
adapter Type check

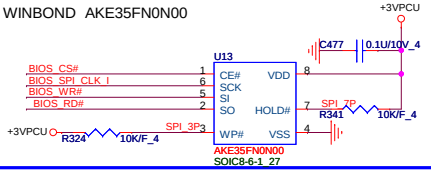


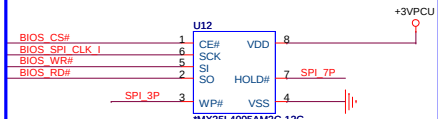


adapter select for EC

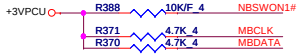
512K byte SPI EC ROM

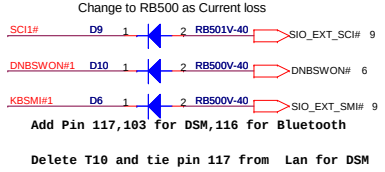
Socket: DG008000031
EON AKE35FN0Q00
WINBOND AKE35FN0N00

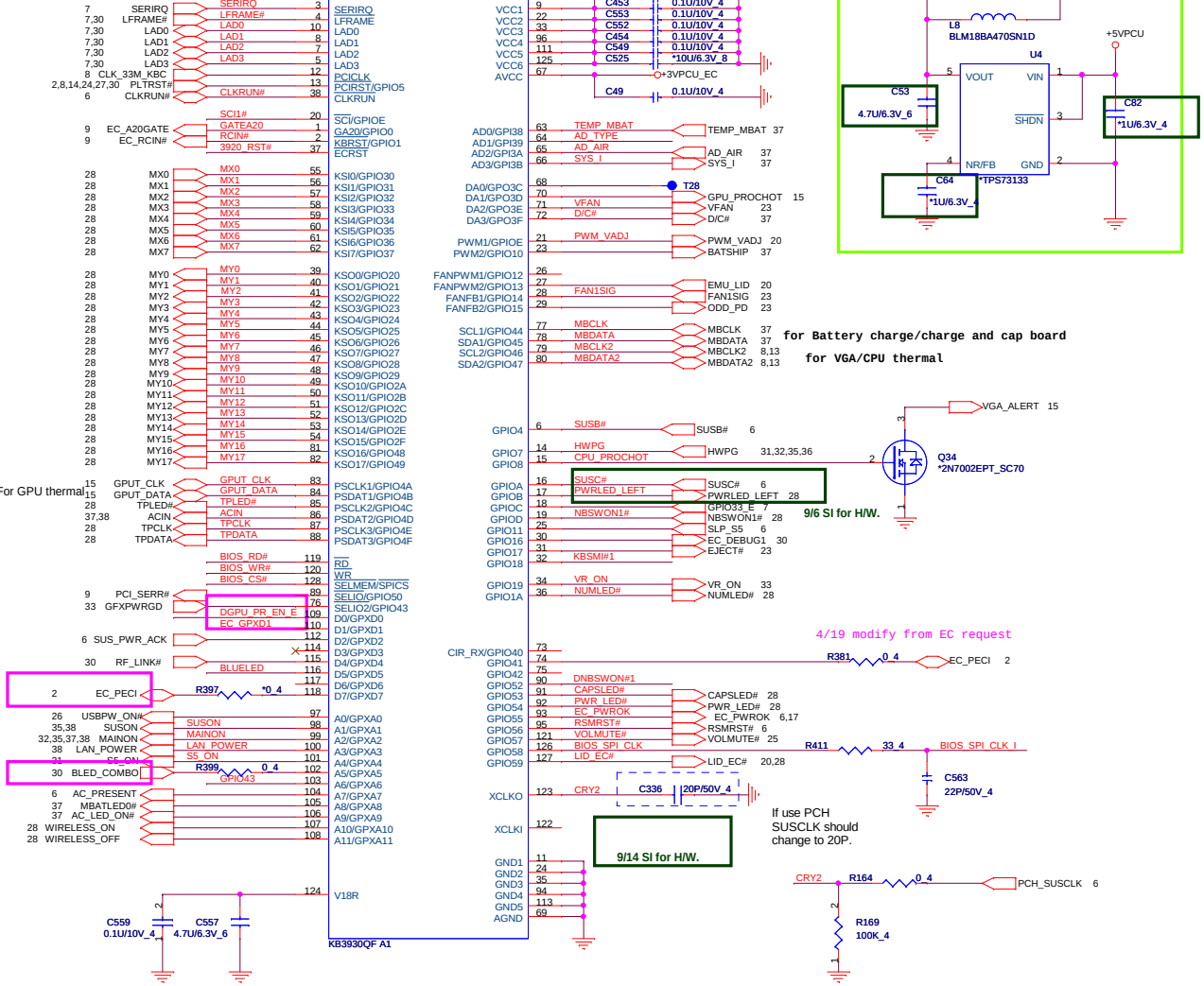


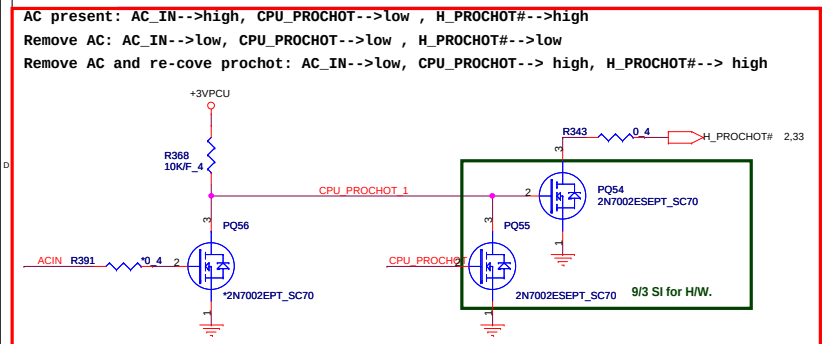


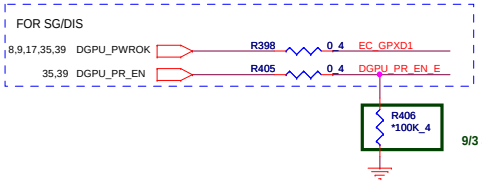
128K byte SPI EC ROM

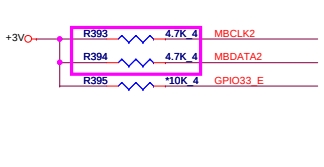


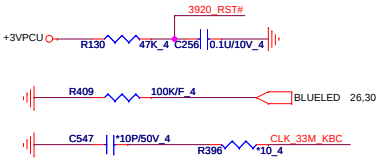












2,4,6,7,8,10,32,33 +1.05V_VTT
2,6,7,8,9,10,12,13,14,17,20,21,22,23,24,25,27,28,30,33,38,39 +3V
7,20,28,31,37 +3VPCU
31,37 +5VPCU

NB5

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	EC (KB3926)/ROM	3A
Date: Saturday, September 18, 2010	Sheet 29 of 39	

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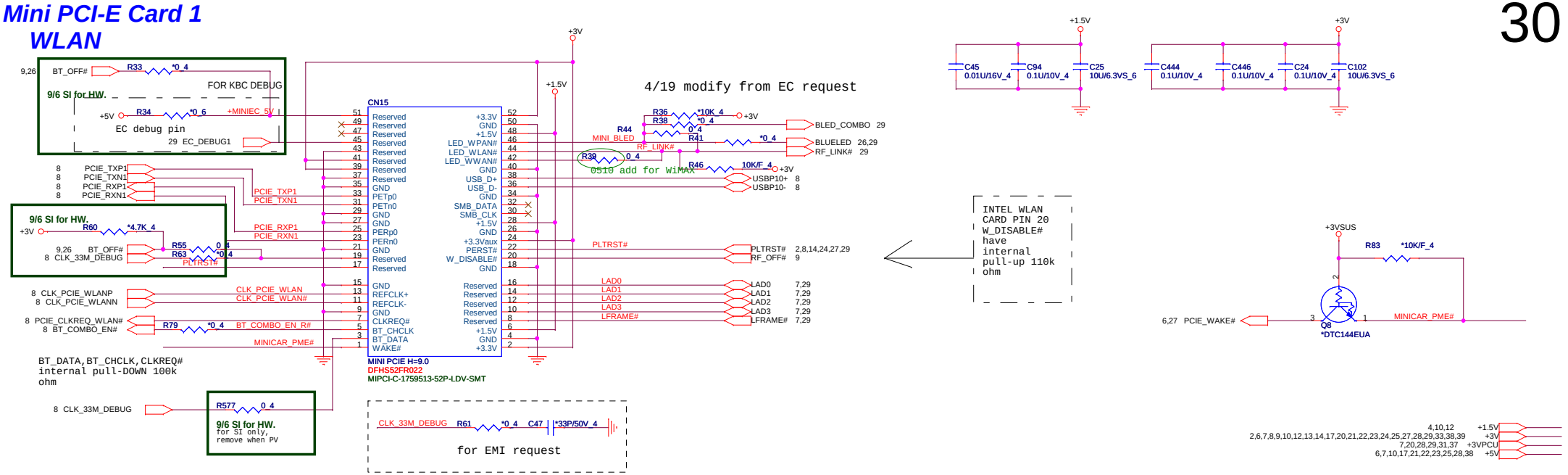
Mini PCI-E Card 1
WLAN



NB5	PROJECT : R13 Quanta Computer Inc.		
	Size: Custom	Document Number: MINI PCIE CONN X1	Rev: 1A
	Date: Saturday, September 18, 2010	Sheet 30 of 39	

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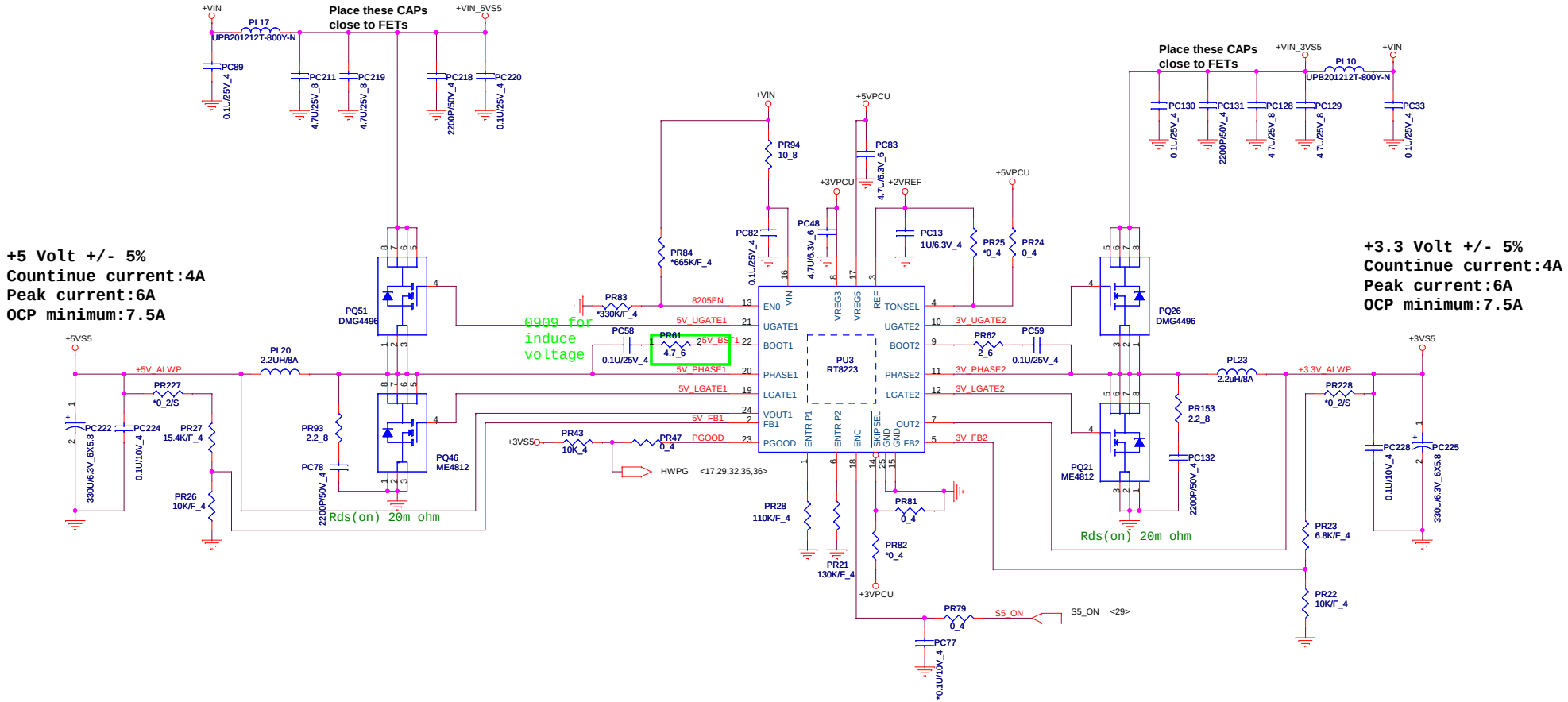

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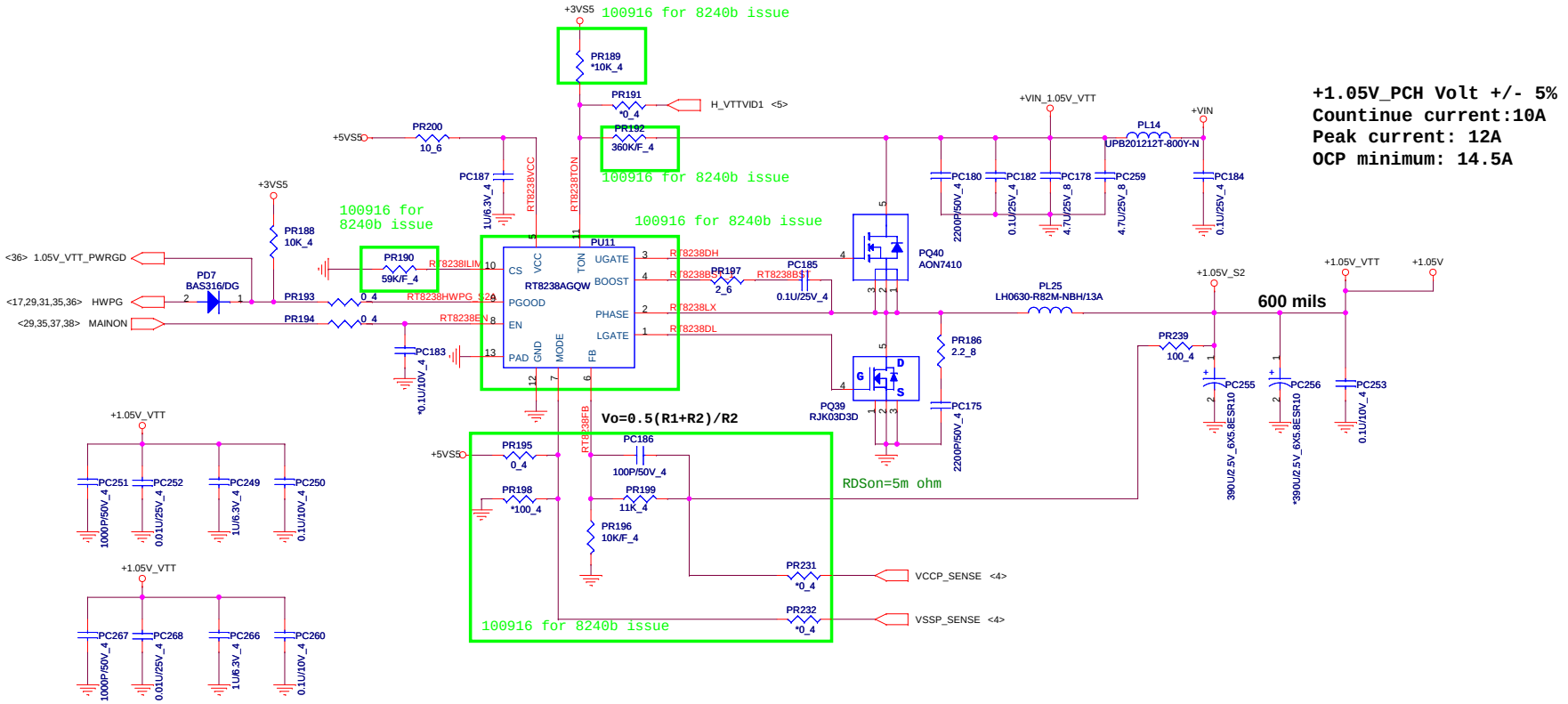

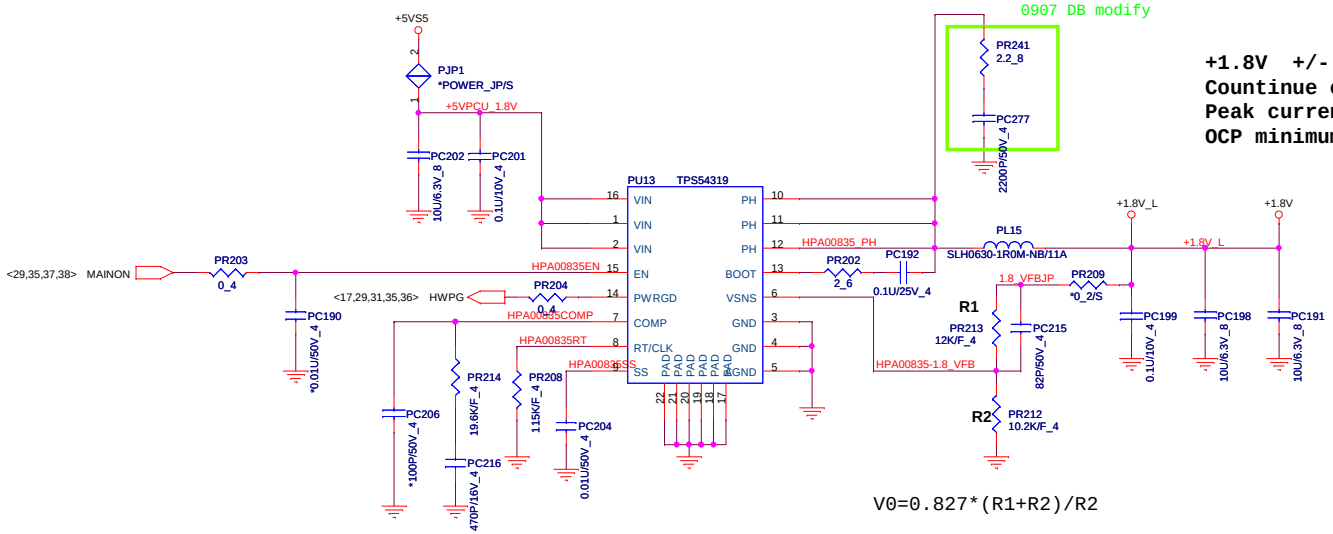

PROJECT : R13
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	+1.1V VTT / PCH	1A

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1.Alert trace routing between data and clock trace
2.Refer to ground
3.Keep out 20 mils

0909 DB MODIFY

B~4350
PUT COLSE TO VCORE Phase 1 Inductor

20100913 for LOAD LINE

SV 35W CPU
VID1=1.05V
IccMax=54A
R_LL=1.9m ohm
OCP~60A

0826 cancel for layout

PUT COLSE TO VCORE HOT SPOT

PUT COLSE TO V_GT HOT SPOT

0907 DB MODIFY

PUT COLSE TO V_GT Inductor

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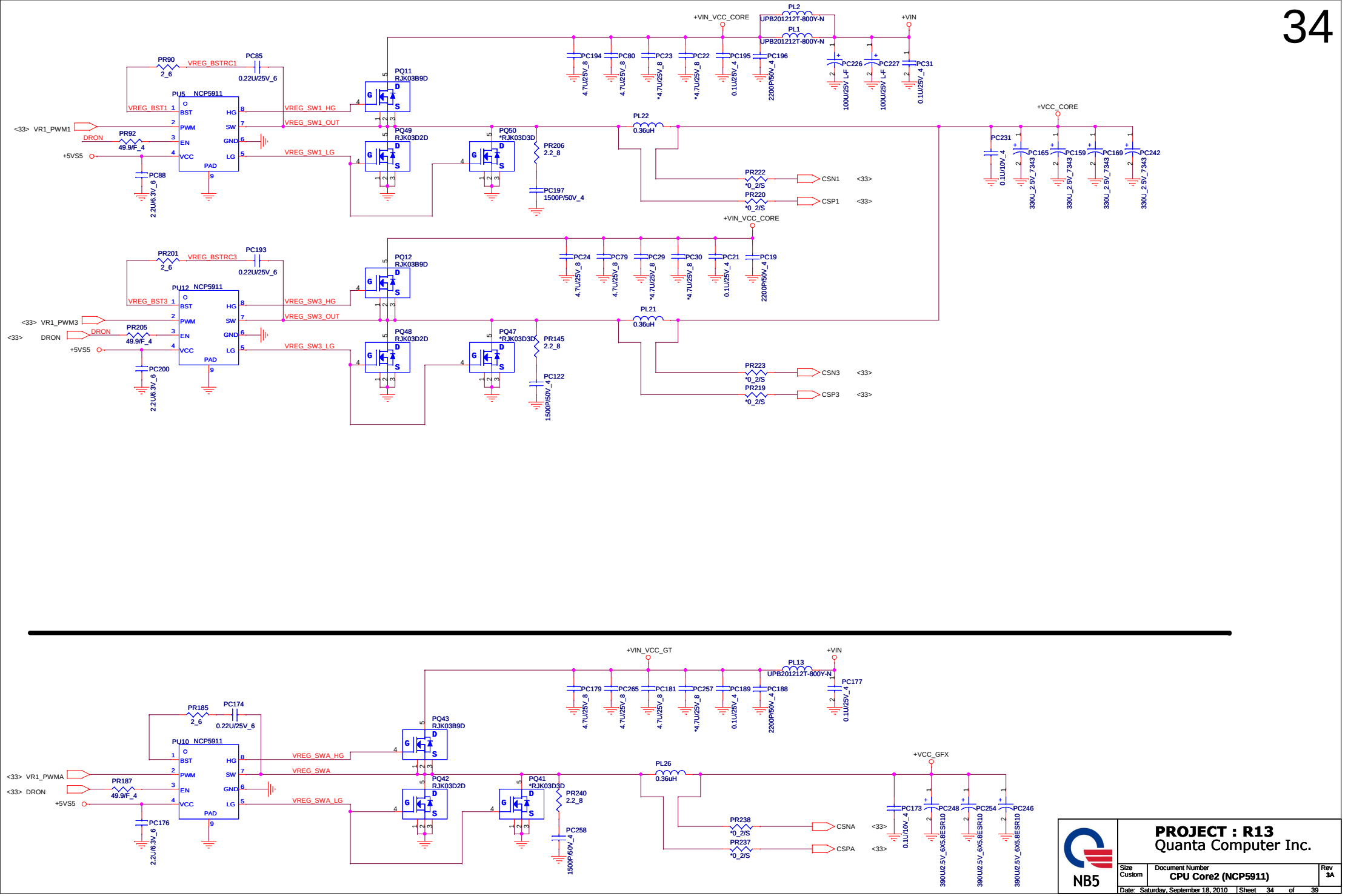
NB5	PROJECT : R13 Quanta Computer Inc.	
Size: Custom	Document Number: CPU Core1 (NCP6131S)	Rev: 1A
Date: Saturday, September 18, 2010	Sheet 33 of 39	



NB5

PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU Core2 (NCP5911)	1A

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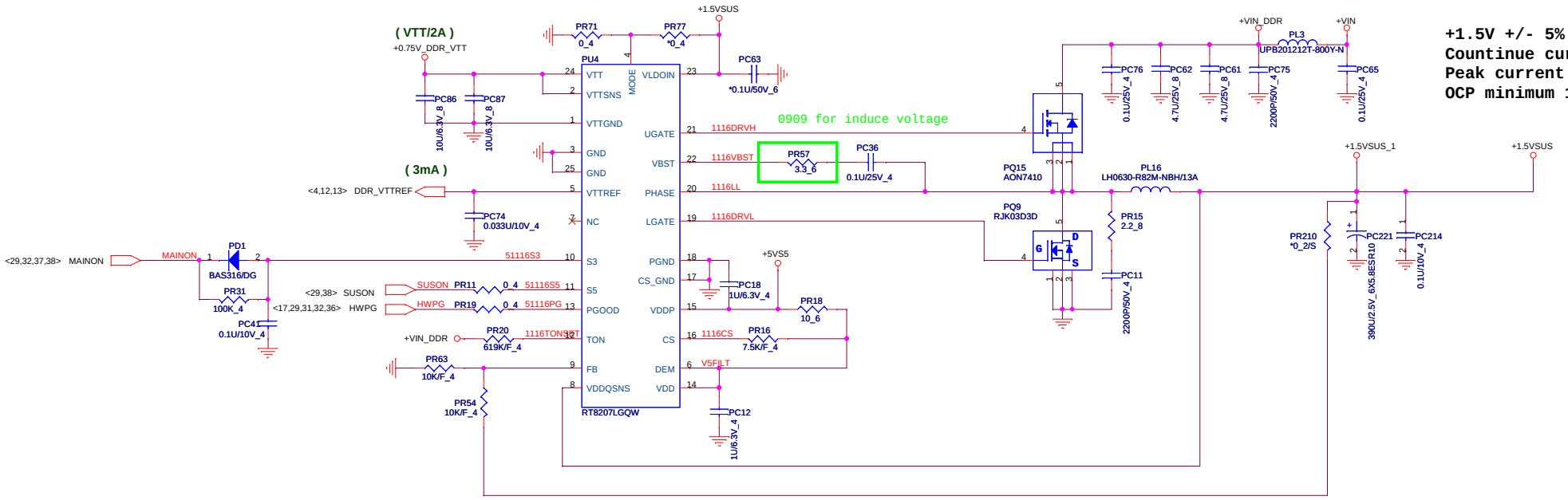
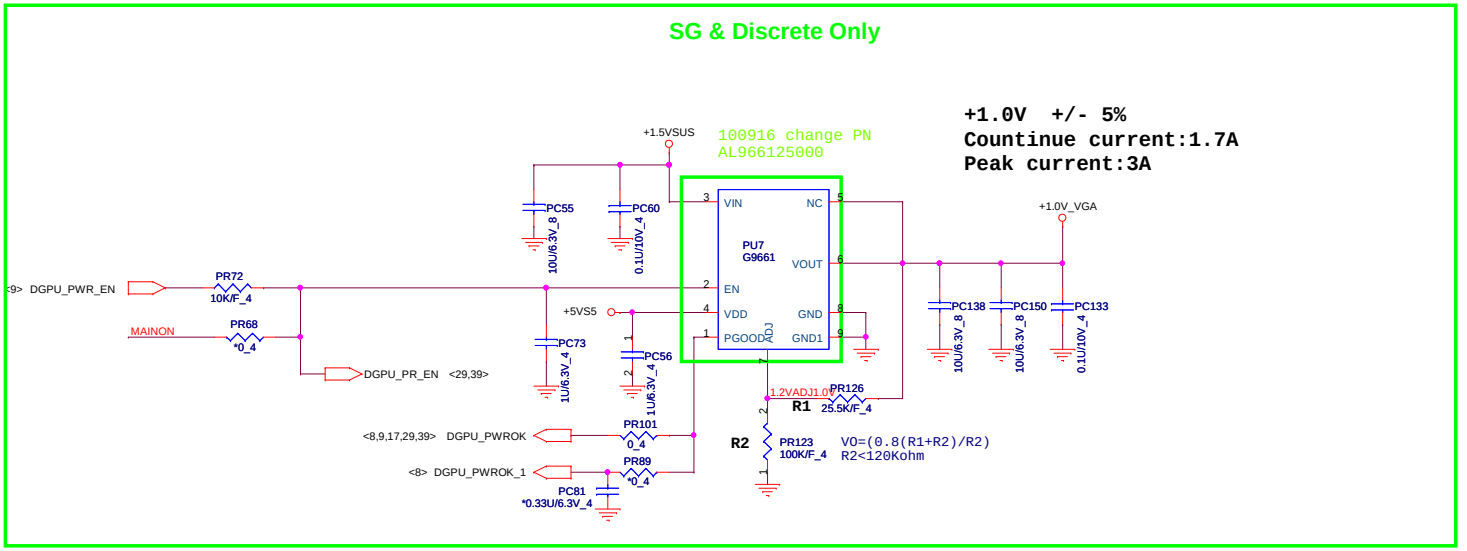


+1.5V +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A

SG & Discrete Only



+1.0V +/- 5%
Countinue current:1.7A
Peak current:3A

PROJECT : R13
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	DDR3 (RT8207)	1A

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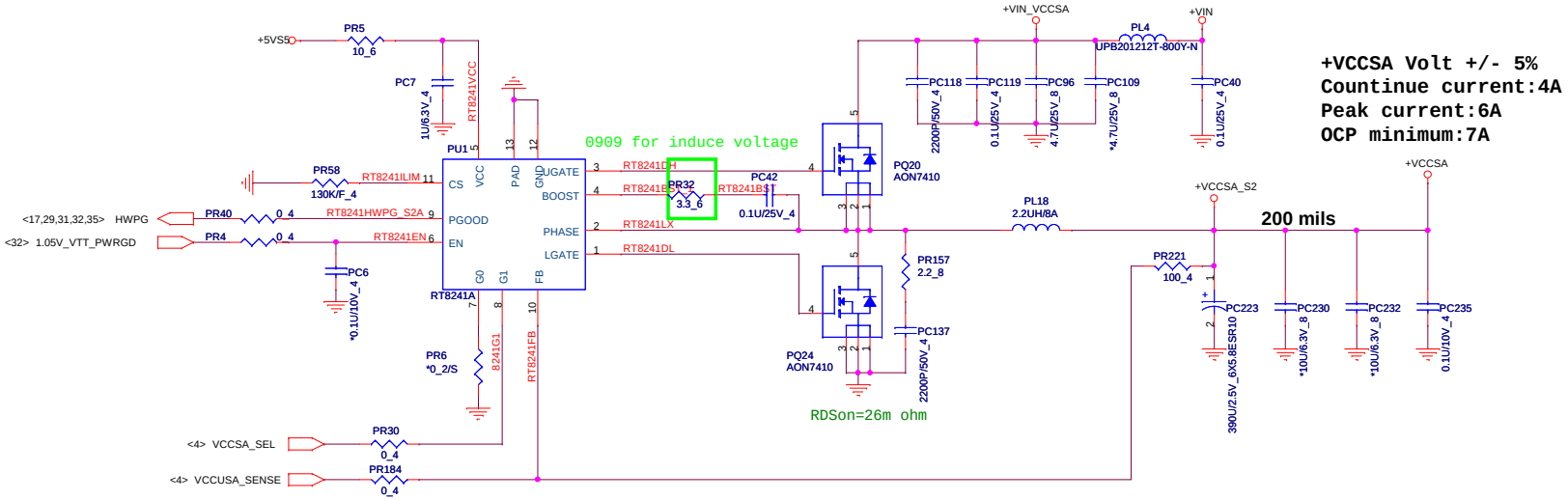

PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.1V VTT / PCH	3A

NB5

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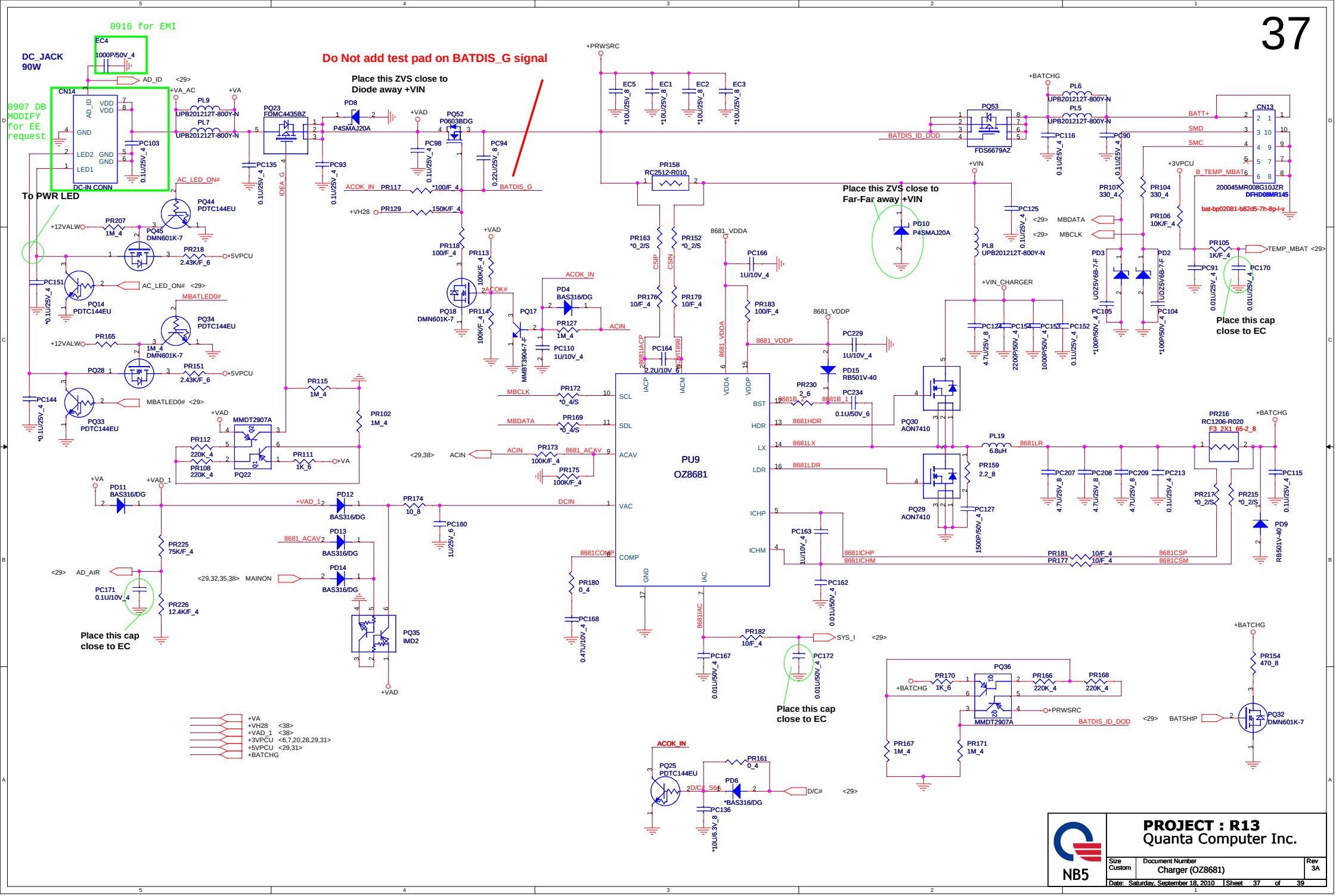
0916 for EMI
DC_JACK
90W
EC4
1000P/50V_4
CN14
AD_ID
VDD
VDD
GND
LED2
GND
GND
LED1
DC-IN CONN
0907 DB MODIFY for EE request
To PWR LED
Do Not add test pad on BATDIS_G signal
Place this ZVS close to Diode away +VIN
Place this ZVS close to Far-Far away +VIN
Place this cap close to EC
Place this cap close to EC
Place this cap close to EC
Place this cap close to EC
PU9
OZ8681
SCL
SDL
ACAV
VAC
COMP
IACP
IACM
VDDA
VDDP
BST
HDR
LX
LDR
ICHP
ICHM
GND
IAC
CSIP
CSIN
PQ23 FDMC4435BZ
PQ52 P0603BDG
PQ53 FDS6679AZ
PQ44 PDTC144EU
PQ45 DMN601K-7
PQ14 PDTC144EU
PQ34 PDTC144EU
PQ33 PDTC144EU
PQ28
PQ18 DMN601K-7
PQ17 MMBT3904-7-F
PQ22 MMDT2907A
PQ30 AON7410
PQ29 AON7410
PQ35 IMD2
PQ25 PDTC144EU
PQ36 MMDT2907A
PQ32 DMN601K-7
PD8 P4SMAJ20A
PD10 P4SMAJ20A
PD4 BAS316/DG
PD11 BAS316/DG
PD12 BAS316/DG
PD13 BAS316/DG
PD14 BAS316/DG
PD6 *BAS316/DG
PD15 RB501V-40
PD9 RB501V-40
PL5 UPB201212T-800Y-N
PL6 UPB201212T-800Y-N
PL7 UPB201212T-800Y-N
PL8 UPB201212T-800Y-N
PL9 UPB201212T-800Y-N
PL19 6.8uH
CN13
BATT+
SMD
SMC
B_TEMP_MBAT
200045MR008G10JZR
DFHD08MR145
bat-bp02081-b82d5-7h-8p-l-v
TEMP_MBAT
+PRWSRC
+VIN
+VIN_CHARGER
+BATCHG
+VAC
+VA
+VAD
+VAD_1
+VH28
+3VPCU
+5VPCU
8681_VDDA
8681_VDDP
8681_VDDA
8681_VDDP
8681HDR
8681LX
8681LDR
8681ICHP
8681ICHM
8681CSP
8681CSM
8681_ACAV
8681IAC
8681COMP
ACOK_IN
ACOK#
ACIN
DCIN
BATDIS_G
BATDIS_ID_DOD
IDEA_G
AC_LED_ON#
MBATLED0#
MBCLK
MBDATA
SYS_I
D/C#
BATSHIP
MAINON
AD_AIR
AD_ID
+12VALW
PR158 RC2512-R010
PR216 RC1206-R020
F3_2X1_65-2_8
PC116
PC90
PC125
PC166
PC229
PC234
PC164
PC110
PC127
PC160
PC162
PC163
PC167
PC168
PC171
PC172
PC180
PC181
PC182
PC136
PR117
PR129
PR163
PR152
PR176
PR179
PR183
PR230
PR159
PR172
PR169
PR173
PR175
PR174
PR225
PR226
PR180
PR182
PR161
PR154
PR167
PR168
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PR218
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PR151
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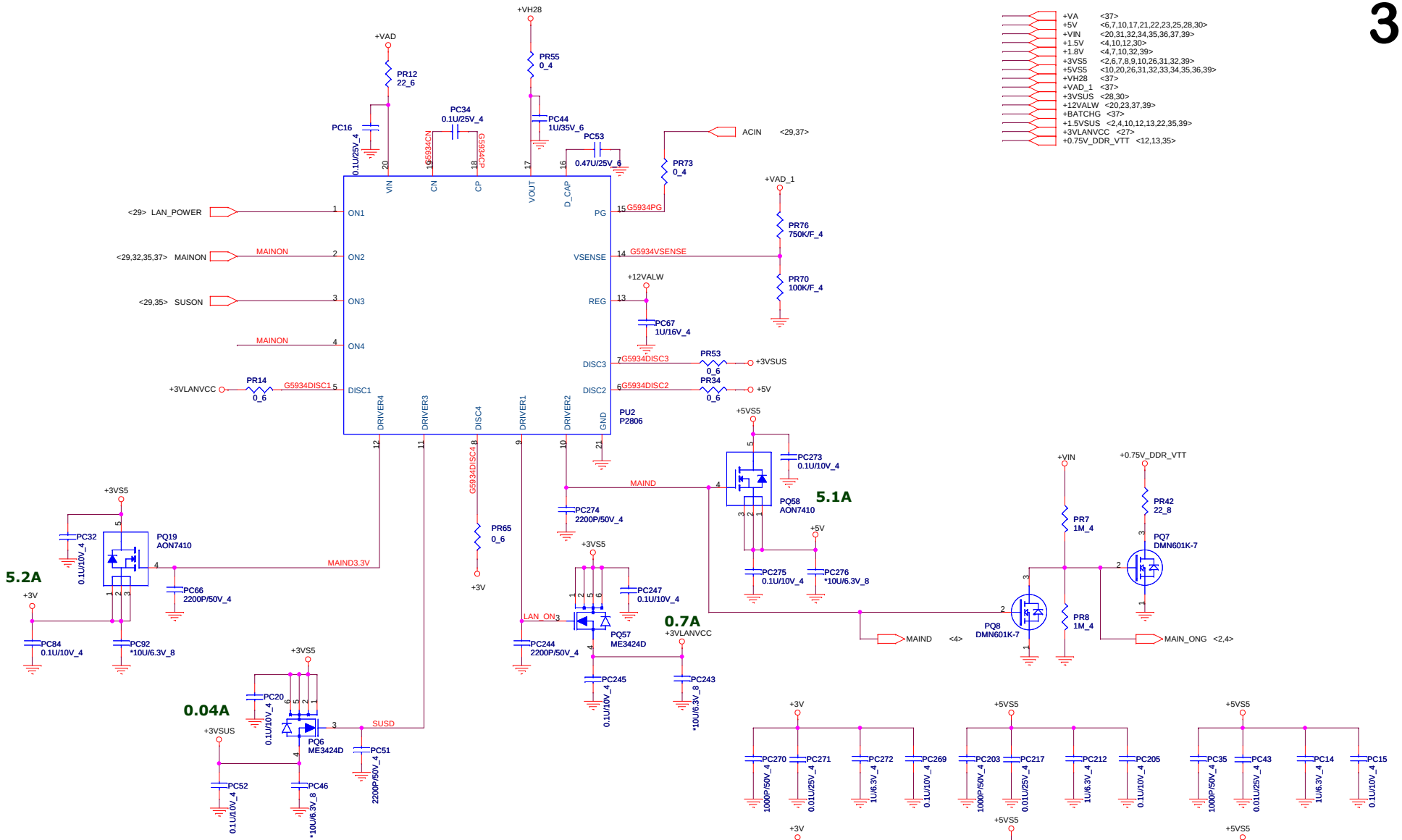
PC221
PC222



PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (G5934)	3A

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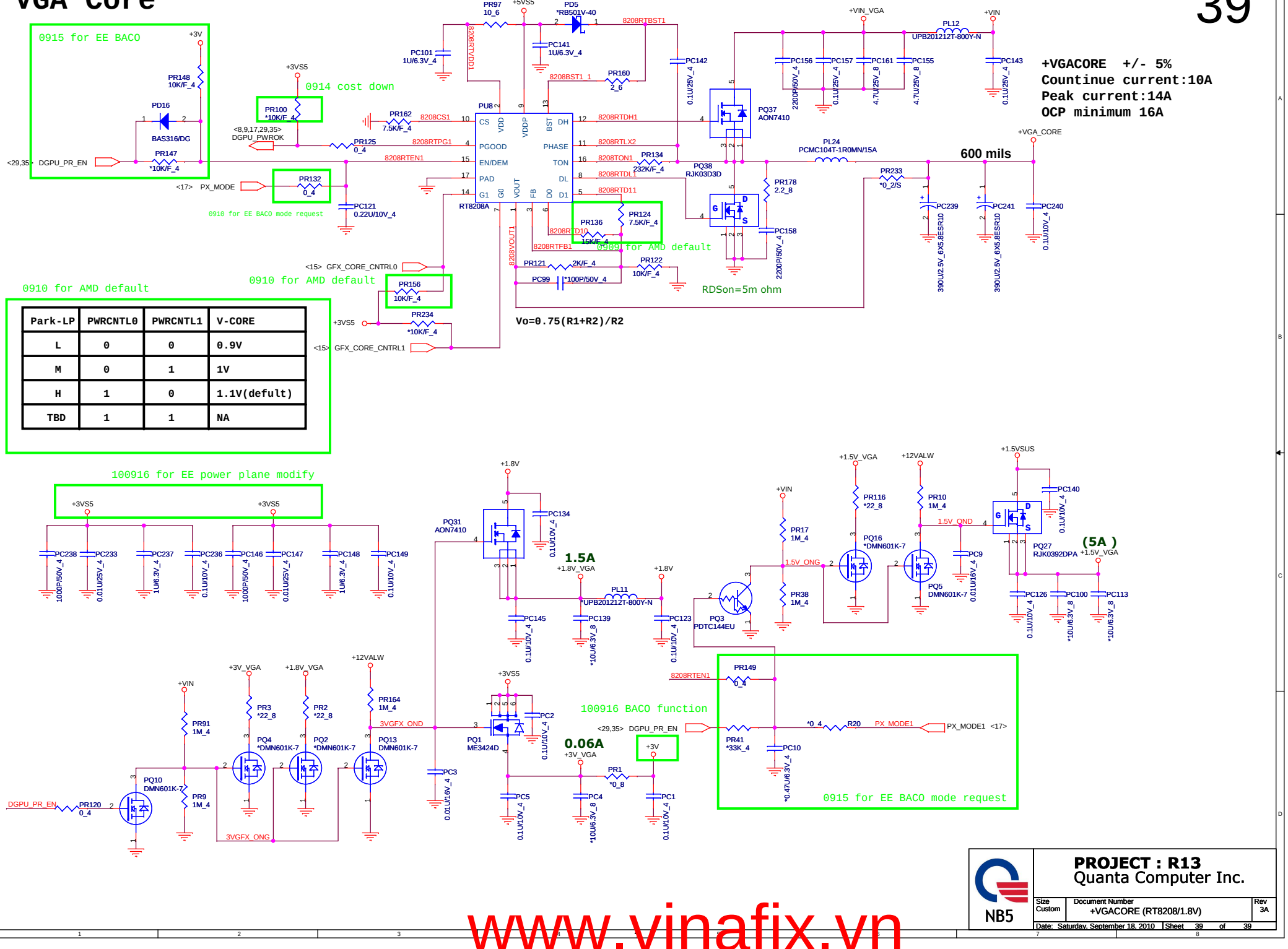
VGA Core



Park-LP	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	1V
H	1	0	1.1V(defult)
TBD	1	1	NA

PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE (RT8208/1.8V)	3A

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